

9212LPJ Series

Clock oscillator, 7.0 x 5.0mm, LVPECL/LVDS/HCSL/LPHCSL Output



REACH and RoHS compliant
Differential output (Non-PLL)
Supply voltage 1.8, 2.5V, 3.3V
Superior phase noise

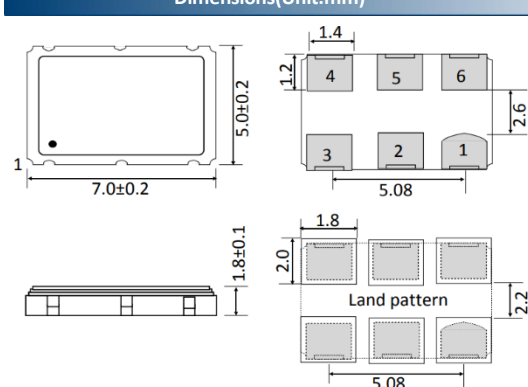


Parameters		Specification	Remarks
Frequency range	F _{nom}	13.5MHz ~ 220.0MHz	
Supply voltage	V _{cc}	1.8V, 2.5V, 3.3V	±5% tolerance; 1.8V LVPECL is not available
Frequency stability	F _{stb}	±25.0ppm, ±50.0ppm, ±100.0ppm	Includes initial tolerance, stability over temperature, Load, V _{cc}
Aging	F _{age}	±3.0ppm max for the 1st year	± 2 ppm (max.) per year thereafter
Operating temperature range (°C)	T _{opr}	-20°C ~ +70°C, -40°C ~ +85°C	
Storage temperature (°C)	T _{stg}	-55°C ~ +150°C	
Output waveform		LVPECL, LVDS, HCSL, LPHCSL	
Output load		Table 1	
Output voltage high	V _{oh}	Table 1	
Output voltage low	V _{ol}	Table 1	
Rise time	T _r	Table 1	
Fall time	T _f	Table 1	
Duty cycle		40%/60%, 45%/55%	
Current consumption	I _{cc}	LVPECL : 30.0mA typical ; 50.0mA max	
		LVDS : 16 mA typical ; 27mA max	
		HCSL : 17.0mA typical ; 30.0mA Max	
		LPHCSL : 11.0mA typical ; 20.0mA Max	
Start-up time	T _{str}	1.0msec max, 5.0msec typical	
Tristate		Pad 1	
Phase noise		Table 2	
Phase jitter (RMS) 12kHz to 20MHz		0.2ps typical ; 0.5ps max for 156.250MHz, 3.3V	0.18 psec (typ.) [For HCLK]
Moisture sensitive level	MSL	1	
ESD sensitive device		Yes	

Table 1. Output characteristics

		LVPECL	LVDS	HCSL	LPHCSL
Output load		50Ω into V _{cc} - 2V	100Ω between outputs	50Ω to GND on each output	None
V _{oh}	Min	V _{cc} - 1.03	1.4 V (typ.)	550mV	550mV
	Max	V _{cc} - 0.6	1.6 V (max.)	850mV	900mV
V _{ol}	Min	V _{cc} - 1.85	0.9 V (min.)	-150mV	-150mV
	Max	V _{cc} - 1.6	1.1 V (typ.)	150mV	150mV
Output swing	Min	595mV	250mV	400mV	550mV
	Typ	750mV	350mV	-	-
Tr/Tf	Max	930mV	450mV	-	-
	Typ	0.3nsec	0.3nsec	0.3nsec	0.4nsec
	Max	0.6nsec	0.5nsec	0.6nsec	0.7nsec

Dimensions(Unit:mm)



Pad 1 : Tri-state
Pad 2 : No connection
Pad 3 : Ground
Pad 4 : Output
Pad 5 : Complimentary
Pad 6 : Supply voltage

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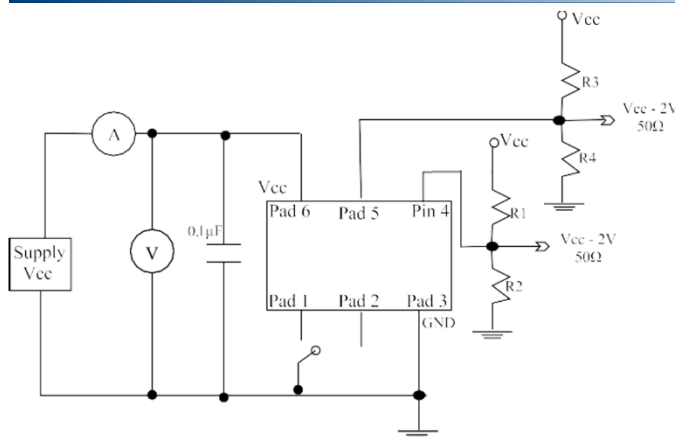


(Phase noise) dBc/Hz typical		
	62.5MHz	156.250MHz
10Hz	-50	-50
100Hz	-82	-80
1kHz	-116	-115
10kHz	-138	-135
100kHz	-144	-142
1MHz	-149	-147

Part number generation									
RLP	2600	B	B	I	S	E	P	L	-PF
ACT series Code	Frequency (MHz)	Frequency stability (±ppm)	Supply voltage (V)	Operating temp. range (°C)	Duty Cycle (%/%)	Output wave	Tristate	Tape & Reel	RoHS Code
RLP	< 100MHz First 4 digit of frequency > 100MHz First 5 digit of frequency Ex. 26.00MHz = 2600 8.00MHz = 0800 14.7456MHz = 1474 156.250MHz = 15625	25 = C 50 = B 100 = A	1.8 = D 2.5 = C 3.3 = B	-20 ~ +70 = B -40 ~ +85 = I	40/60 = S 45/55 = H	LVPECL = M LVDS = K HCSL = S LPHCSL = L	Tristate = P	Loose = L 1000 = C 3000 = D	-PF

Note: 1.8V LVPECL is not available. It is important to suffix the above part number with full frequency required to give a completed part number as illustrated below. Full Example part number : **RLP2600BBISMPL-PF [26MHz]**, **RLP1474BBISMPL-PF [14.7456MHz]**

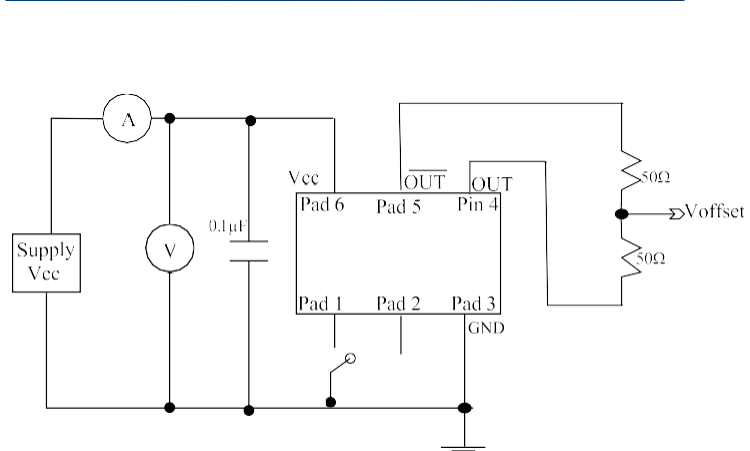
LVPECL Test circuit



LVPECL Resistor values

Vcc	R1, R3	R2, R4
+3.3V	127Ω	82.5Ω
+2.5V	250Ω	62.5Ω

LVDS Test circuit

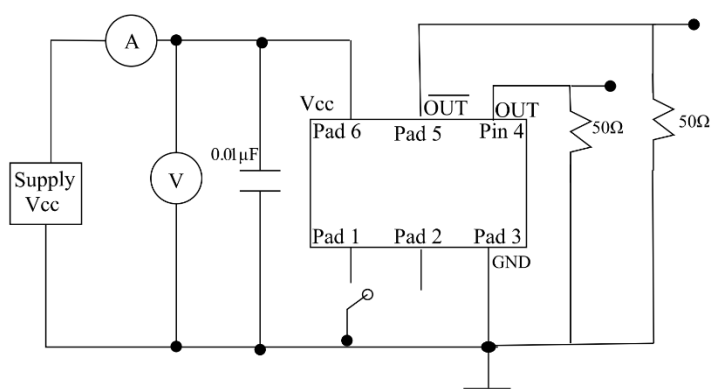


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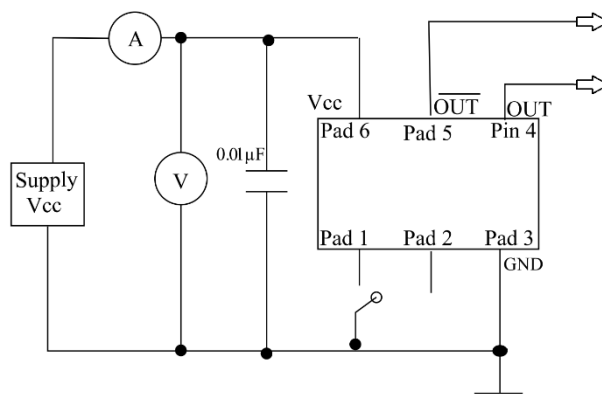
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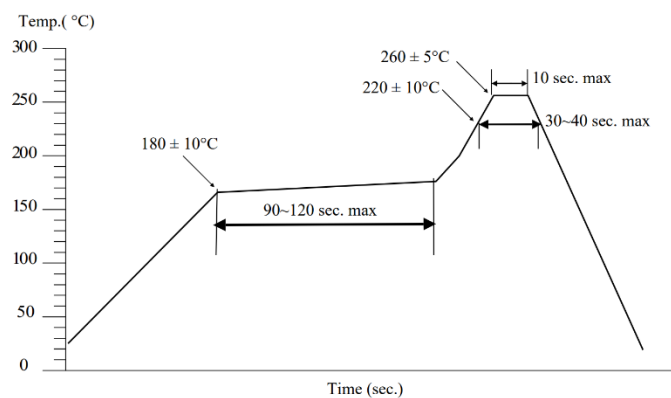
HCSL Test circuit



LPHCSL Test circuit



Solder reflow profile



Drawing control: (Internal use only)
Commodity code:
854370 90 45 for 1.8MHz < F < 67MHz
854370 90 99 for < 1.8MHz and > 67MHz
Issue number : N2
Date : 30/06/2026
Internal reference : M6