ARTC-4040 Low Power Consumption SOP8/TSSOP8 I²C RTC

1 Overview

The ARTC-4040 is an I²C bus interface real-time clock with a low power consumption. It supports calendar (Century, year, month, day, hour, minute, second), timer and alarm function. The SOP8/TSSOP8 package makes it suitable for use in portable electronic devices.

Manufacture Part Number	Product Name	Description
ARTC-4040-LP-PF	ARTC-4040	-40℃~85℃，External 32K Crystal, SOP8
ARTC-4040-LPT-PF	ARTC-4040	-40℃~85℃，External 32K Crystal, TSSOP8

2 Block Diagram

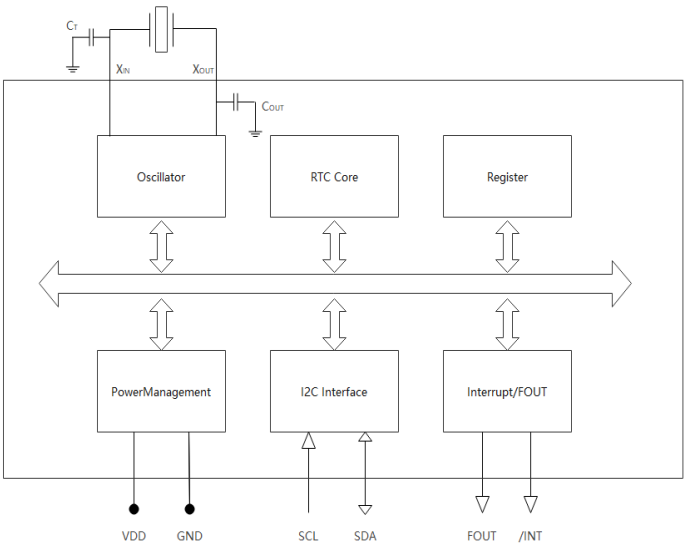
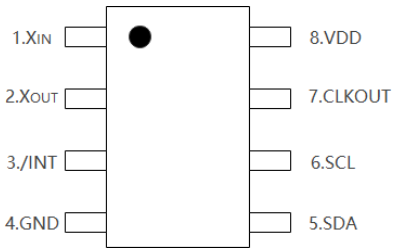


Figure 1. Block Diagram

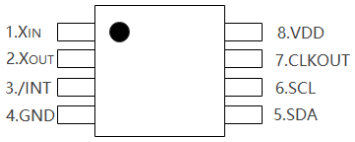
3 Features

- Low Current Consumption: 0.9uA (Typ.)
- Communication Interface: I²C bus
- Alarm, Timer and Interruption functions
- Frequency Output
- External 32K crystal
- RoHS & REACH compliant
- Integrated Oscillator Capacitors
- Power Supply Voltage: 1.2V ~ 5.5V
- Leap Years Autocorrection
- Operation Temperature Range: -40°C ~ +85°C
- Package: 4.9 * 6.0 * 1.6mm (SOP8)
  Package: 3.0 * 4.9 * 1.1mm (TSSOP8)

4 Pin Definition



SOP8 PIN CONFIG



TSSOP8 PIN CONFIG

Table 1. Pin Definition

Pin Number	Pin Name	I/O	Description
1	X_{IN}		Oscillator Input, must be connected to an 8pf~25pf capacitor for trimming.
2	X_{OUT}		Oscillator Output.
3	/INT	Out	Alarm, Timer Output. (Open-Drain).
4	GND	-	Ground
5	SDA	In/Out	I2C data signal
6	SCL	In	I2C clock signal
7	CLKOUT	Out	Frequency Output. (Open-Drain).
8	V_{DD}	-	Power in

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
I/O Input Voltage	V_{IN}	GND-0.3		6.5	V	SCL, SDA Input
Clock Output Voltage	V_{OUT}	GND-0.3		6.5	V	SDA，/INT Output, FOUT
Storage Temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage (normal mode)	V_{DD}	1.6	3.0	5.5	V	Note1,2,3
Power Supply Voltage (Time keeping)	V_{DD}	1.2	3.0	5.5	V	
Operation Temperature	T_{OPR}	-40	25	85	℃	

Note:

1: V_{DD} needs to be at least 2.5V for the oscillator to work in a stable manner.

2: A capacitor(8pf~25pf) needs to be connected between X_{IN} and GND.

3: Ensure that the ramp up time of the power supply from 0 to VDD is less than 100ms.

5.3 Oscillator Characteristics

Table 4. Oscillator Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Oscillator						
X_{out} Capacitor	C_{OUT}	15	25	35	pF	
External Crystal(32.768KHz)						
Series Resistance	R_S			100	kΩ	
Capacitor Trim	C_T	8		25	pF	
Load Capacitance	C_L	7		12.5	pF	$C_L=\frac{C_T*C_{OUT}}{C_T+C_{OUT}}$
FOUT Duty cycle	t_w/t	40	50	60	%	FOUT

5.4 DC Characteristics

Table 5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current1	I_{DD1}		1.0	3.0	uA	V_{DD}=5.0V	f_{SCL} = 0 Hz, /INT = OFF, FOUT = OFF, SDA="L", SCL="L"
Average Current2	I_{DD2}		0.9	2.8		V_{DD}=3.0V	
Average Current3	I_{DD3}		1.9	3.8		V_{DD}=5.0V	FOUT = 32.768KHz (CL=15PF), /INT=OFF , SDA="L", SCL="L"
Average Current4	I_{DD4}		1.7	3.5		V_{DD}=3.0V	
Input High Voltage	V_{IH}	0.8*V_{DD}		5.5	V	SCL， SDA	
Input Low Voltage	V_{IL}	GND		0.2*V_{DD}	V		
Output Low Voltage	V_{OL1}	GND		GND+0.25	V	VDD =5V, IOL=1mA	/INT
	V_{OL2}	GND		GND+0.4		VDD =3V, IOL=1mA	
	V_{OL3}	GND		GND+0.5		VDD =5V, IOL=1mA	FOUT
	V_{OL4}	GND		GND+0.3		VDD =3V, IOL=0.5mA	
Input Leak Current	I_{LK}	-0.1		0.1	uA	SDA, SCL， V_{IN} = V_{DD} or GND	
Output Leak Current	I_{OZ}	-0.1		0.1	uA	SDA, V_{IN} = V_{DD} or GND	

5.5 AC Characteristics

Table 6. AC Characteristics

V_{DD}=1.6V～5.5V; Ta=-40℃～+85℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL Low Voltage Time	t_{LOW}	1.3			us
SCL How Voltage Time	t_{HIGH}	0.6			us
Start condition hold time	$t_{HD;\ STA}$	0.6			us
Start condition setup time	$t_{SU;\ STA}$	0.6			us
Stop condition setup time	$t_{SU;\ STO}$	0.6			us

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;\ DAT}$	100			ns
Data hold time	$t_{HD;\ DAT}$	0			ns
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

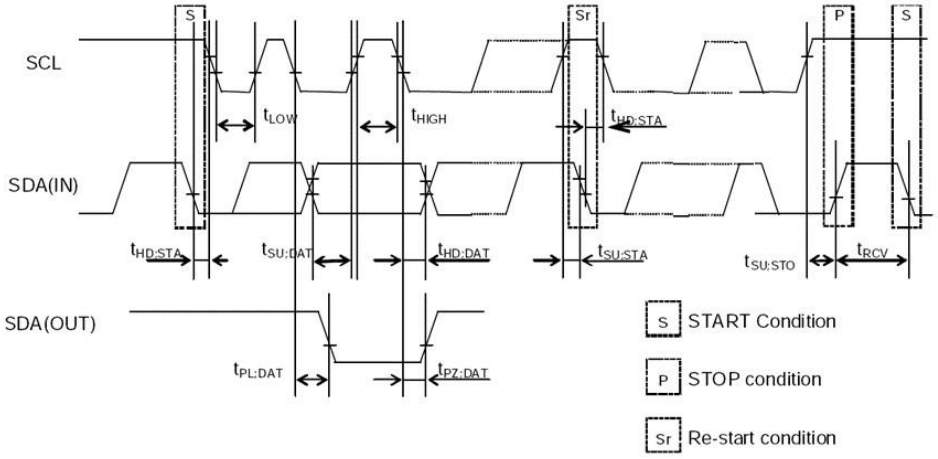


Figure 2. I²C bus Timing Chart

Note: When the master device gets access to this slave device through the I2C, it should complete the whole operation in less than 1s, otherwise it will be reset by the I2C bus through the internal bus overtime function.

6 Registers

6.1 Register Lists

Address 0x00~0x01: Control and Flag Registers Group

Address 0x02~0x08: Time Register Group

Address 0x09~0x0C: Alarm Register Group

Address 0x0D: CLKOUT Control Register

Address 0x0E~0x0F: Timer Register Group

Address 0x11: Offset Register

Table 7. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x00	Control Register_1	EXT_TEST	○	STOP	○	○	○	○	○	R/W
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	R/W
0x02	SEC	VLF	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x03	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x04	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x05	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x06	WEEK	○	○	○	○	○	BCD code, Week ones place, 0-6			R/W
0x07	MONTH	Century	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x08	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x09	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x0a	HOUR Alarm	AE	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x0b	DAY Alarm	AE	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x0c	WEEK Alarm	AE	○	○	○	○	BCD code, Week ones place, 0-6			R/W
0x0d	CLKOUT_Control Register	FE	○	○	○	○	○	FD[1:0]		R/W
0x0e	Timer_Control Register	TE	○	○	○	○	○	TD[1:0]		R/W
0x0f	Timer Counter	128	64	32	16	8	4	2	1	R/W
0x11	Offset Control	MODE	OFFSET_CFG[6:0]							R/W

Note:

1, After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers before using the RTC.

2. The default value of register after power on:

Initial 0: AF、TF、AIE、TIE、FD[1:0]、TD[1:0].

Initial 1: VLF、AE、FE、TE.

3. The bits marked with “○” can be read out “0” after initializing.

4. Only 0 can be written to TF、AF and VLF bits.

6.2 Details of Registers

6.2.1 Clock counter registers

Table 8. Second, Minute and Hour Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x02	SEC	VLF	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x80
0x03	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x04	HOUR	○	○	BCD code, Hour tens place, 0-2		0x00				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

VLF（Voltage Low Flag）：Voltage Low Flag, when voltage is lower than 1.3V, this bit will be set to”1” and kept at this value until changed to “0” by software.

Table 9. Day Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x05	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if it’s a leap year or not.

Table 10. DAY Register Value Range

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

Table 11. Week Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x06	WEEK	○	○	○	○	○	BCD code, Week ones place, 0-6			0x00

Table 12. WEEK Register Value table

	Bit2	Bit1	Bit0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 13. Month and Year Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x07	MONTH	Century	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
0x08	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value1~12

YEAR: BCD format, Value01~99(2001~2099)

Century: 0-Century is X, 1-Century is X+1

Example: 2023/01/01 Wednesday 21:18:36

Table 14. Example of time setting

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x02	SEC	○	0	1	1	0	1	1	0
0x03	MIN	○	0	0	1	1	0	0	0
0x04	HOUR	○	○	1	0	0	0	0	1
0x05	DAY	○	○	0	0	0	0	0	1
0x06	WEEK	○	○	○	○	○	0	1	1
0x07	MONTH	○	○	○	0	0	0	0	1
0x08	YEAR	0	0	1	0	0	0	1	1

6.2.2 Alarm registers

Table 15. Alarm Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	0x00
0x09	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x80
0x0a	HOUR Alarm	AE	○	BCD code, Hour tens		BCD code, Hour ones place, 0-9				0x80

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
				place, 0-2						
0x0b	DAY Alarm	AE	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x80
0x0c	WEEK Alarm	AE	○	○	○	○	BCD code, Week ones place, 0-6			0x80

Alarm interruption can be generated by setting these registers and the cooperation of AIE and AF. AE（Alarm Enable）：Alarm Enable bit，0-Enable；1-Disable.

AF function refer to 0x01 register bit3.

AIE function refer to 0x01 register bit1.

6.2.3 Timer registers

Table 16. Timer Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	0x00
0x0e	Timer_Control Register	TE	○	○	○	○	○	TD[1]	TD[0]	0x80
0x0f	Timer Counter	128	64	32	16	8	4	2	1	0x00

Timer interruption can be generated by setting these registers and the cooperation of TE、TF 、TIE and TD[1:0]. TI_TP: select interrupt output mode: 1-Pulse output mode, 0- Level output mode.

TE function refers to 0x0e register bit7. TF function refers to 0x01 register bit2. TIE function refers to 0x01 register bit0.

TD[1:0] function refers to 0x0e register bit1 and bit0.

6.2.4 CLKOUT control registers

Table 17. CLKOUT Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0D	CLKOUT_Control Register	FE	○	○	○	○	○	FD[1]	FD[0]	0x80

Used for the CLKOUT Frequency function.

FE（Fout Enable）：0- Disable CLKOUT Frequency function, 1-Enable CLKOUT Frequency function。

FD[1]，FD[0] to configure the output frequency. As shown in the below table：

Table 18. FD Table

FD [1]	FD [0]	CLKOUT Frequency
0	0	32768Hz Output
0	1	1024Hz output
1	0	32Hz output
1	1	1Hz Output

6.2.5 Timer control registers

Table 19. Timer Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0E	Timer_Control Register	TE	○	○	○	○	○	TD[1]	TD[0]	0x80

Used for the specified functions, including Time Update Interruption.

TE（Timer Enable）：0- Disable Timer Interrupt function, 1-Enable Timer Interrupt function。

TD[1]，TD[0]：Timer/Counter Clock configuration bits, just as below table：

Table 20. TD Table

TI_TP	TD [1]	TD [0]	Timer/Counter Clock	Interruption duration Timer Counter = 1	Interruption duration Timer Counter > 1
1	0	0	4096Hz（244.14us）	1/8192	1/4096
1	0	1	64Hz（15.625ms）	1/128	1/64
1	1	0	1Hz（Second）	1/64	1/64
1	1	1	1/60Hz（Min）	1/64	1/64

Recommended steps: (Use timer for the first time / Changing timer counter when timer is active)

1) Set TE=0, TF=0, TIE=0
2) Set TD[1:0]=b'00, delay 200us
3) Write TI_TP according to customer needs
4) Write timer counter (Reg0x0F) according to customer needs
5) Write timer clock (TD[1:0]) according to customer needs
6) Set TE=1, TIE=1

6.2.6 Control register

Table 21. Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00	Control Register_1	EXT_ TEST	○	STOP	○	○	○	○	○	0x00
0x01	Control Register_2	○	○	○	TI_TP	AF	TF	AIE	TIE	0x00

EXT_TEST: 1:Test Mode, 0: Normal Mode.

STOP: 1: RTC Clock is Stop, 0: RTC Clock is normal.

AF（Alarm Flag）：Alarm Flag, when an Alarm Interruption is generated, this bit will change from "0"to "1",and be kept at this value until changed to "0" by software;

TF（Timer Flag）：Timer Flag, when timer interruption is generated, this bit will change from “0”to “1”,and be kept at this value until changed to “0” by software;

AIE（Alarm Interrupt Enable）：When AF changes from“0”to“1”，this bit can control if the interruption generates or not. 0-Do not generate（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

TIE（Timer Interrupt Enable）：When TF changes from“0”to“1”，this bit can control if the interruption generates or not. 0-Do not generate（/INT maintain high resistance），1-generate the interruption（/INT changes from high resistance to low voltage）。

6.2.7 Offset control register

Table 22. Offset Control Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x11	Offset Control	MODE	OFFSET_CFG[6:0]							0x00

Mode: Offset mode bit. See below table

Offset_cfg [6:0]: For MODE = 0, each LSB introduces an offset of 4.069 ppm. For MODE = 1, each LSB introduces an offset of 4.34 ppm. The offset value is coded in two complements giving a range of +63 LSB to –64 LSB. See below table.

Table 23. Mode

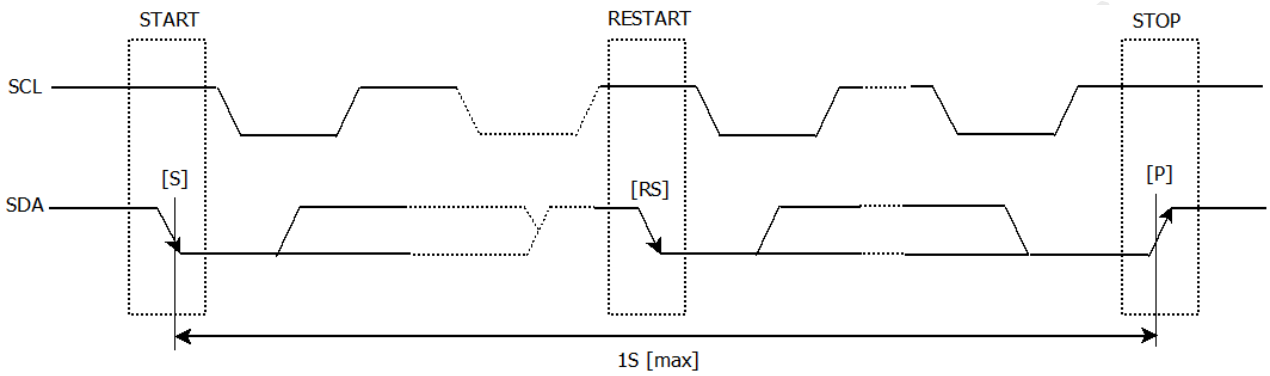
Symbol	Value	Description
Mode	0	Offset is made once every 4 minutes
	1	Offset is made once every 2 hours

Table 24. Offset_Cfg

Offset_cfg[6:0]	Offset value in decimal	Offset value in ppm	
		Mode 0	Mode 1
011 1111	+63	-256.347	-273.42
011 1110	+62	-252.278	-269.080
……	……	……	……
000 0010	+2	-8.138	-8.680
000 0001	+1	-4.069	-4.34
000 0000	0	0	0
111 1111	-1	+4.069	+4.34

111 1110	-2	+8.138	+8.680
……	……	……	……
100 0001	-62	+252.278	+269.080
100 0000	-63	+256.347	+273.42

7 I²C Bus Interface



The I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. The I²C bus device can be defined as “Master” and “Slave”. ARTC-4040 can only be used as a Slave.

7.1 Cautions

The I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second in case the bus is set to standby mode automatically. If the time is more than 1s, the ARTC-4040 will reset the I²C Interface.

ARTC-4040’s I²C bus interface supports single byte read/write operations as well as multiple byte incremental access. After address 0xFF, the next one will be 0x00.

7.2 Slave Address

Table25. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A3h (Read)	1	0	1	0	0	0	1	1 (Read)
A2h (Write)								0 (Write)

ARTC-4040I²C bus Slave Address is [1010 001*].

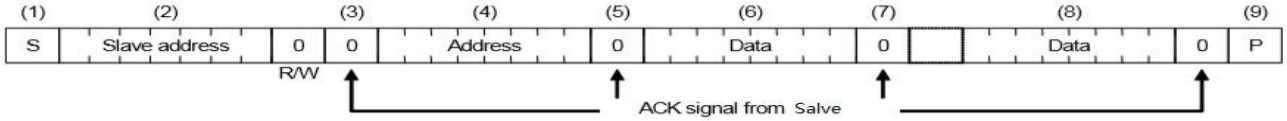
7.3 I²C bus protocol

It is assumed that the CPU is the master and ARTC-4040 is the slave in this section.

7.3.1 Write process

The I²C bus includes an address auto-increment function, once the initial address has been specified, the ARTC-4040 increments (+1) to the address automatically after each data batch is sent, then writes the next batch of data.

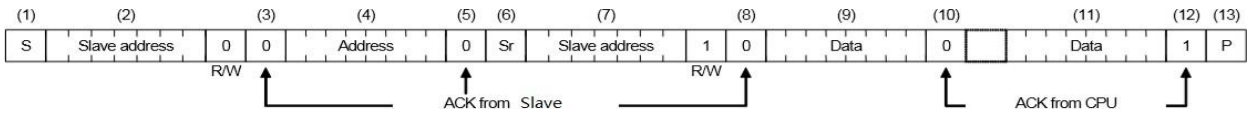
(1) CPU sends start condition[S]
(2) CPU sends ARTC-4040's slave address a R/W bit to set to write mode
(3) CPU verifies ACK signal from ARTC-4040
(4) CPU sends write address to ARTC-4040
(5) CPU verifies ACK signal from ARTC-4040
(6) CPU sends write data to the address specified in step (4)
(7) CPU verifies ACK signal from ARTC-4040
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



7.3.2 Read process

Writing to the address should be done with write mode first, then reading the data should be done with read mode.

(1) CPU sends start condition[S]
(2) CPU sends ARTC-4040's slave address a R/W bit to set to write mode
(3) CPU verifies ACK signal from ARTC-4040
(4) CPU sends address for reading from ARTC-4040
(5) CPU verifies ACK signal from ARTC-4040
(6) CPU sends RESTART condition [Sr]
(7) CPU sends ARTC-4040's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from ARTC-4040
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

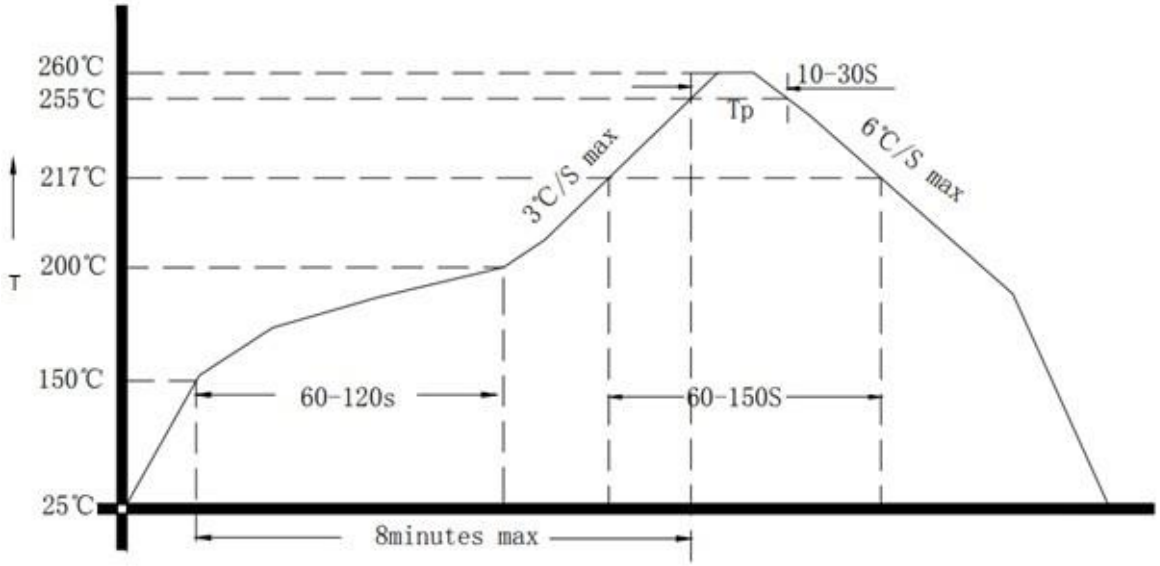
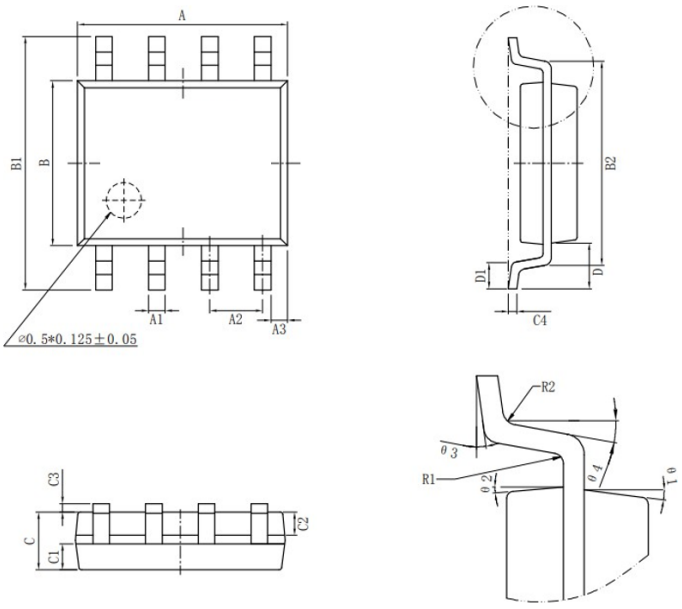


Figure 3. Reflow Soldering Curve

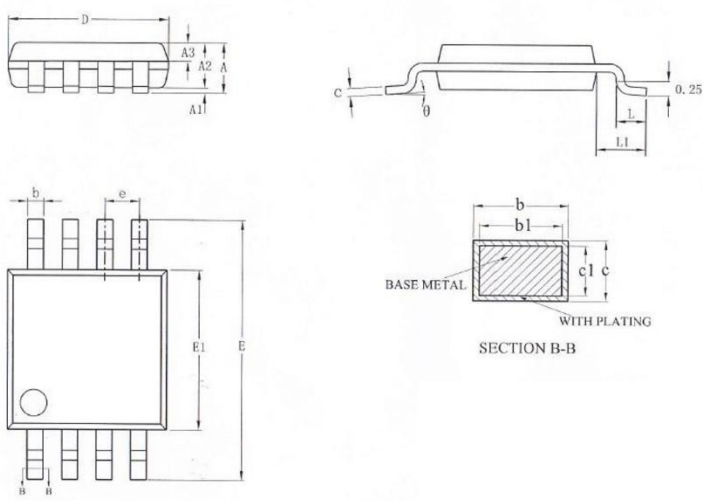
Note: It is recommended to solder the IC under the conditions shown in the curve above. You must pay attention to the temperature and time under heat when manual soldering. If the temperature is over +260℃, you will worsen the XO performance or even damage it.

9 Dimensions and Marking



SOP8 Dimension and Mark

SOP8 Dimension/mm	Min.	Typ.	Max.
A	4.8	4.9	5.0
A1	0.356	--	0.456
A2	--	1.27	--
A3	--	0.345	--
B	3.8	3.9	4.0
B1	5.8	6.0	6.2
B2	--	5.00	--
C	1.3	--	1.6
C1	0.55	--	0.65
C2	0.55	--	0.65
C3	0.05	--	0.20
C4	0.203	--	0.233
D	--	1.05	--
D1	0.4	--	0.8
R1	--	0.2	--
R2	--	0.2	--
θ1	17°		
θ2	13°		
θ3	0°~8°		
θ4	4°~12°		



TSSOP8 Dimension and Mark

TSSOP8 Dimension/mm	Min.	Typ.	Max.
A	--	--	1.1
A1	0.05	--	0.15
A2	0.75	0.85	0.95
A3	0.3	0.35	0.4
b	0.28	--	0.36
b1	0.27	0.30	0.33
c	0.15	--	0.19
c1	0.14	0.15	0.16
D	2.9	3.0	3.1
E	4.7	4.9	5.1
E1	2.9	3.0	3.1
e	0.65BSC		
L	0.4	--	0.7
L1	0.95REF		
θ	0°	--	8°

10 Package Information

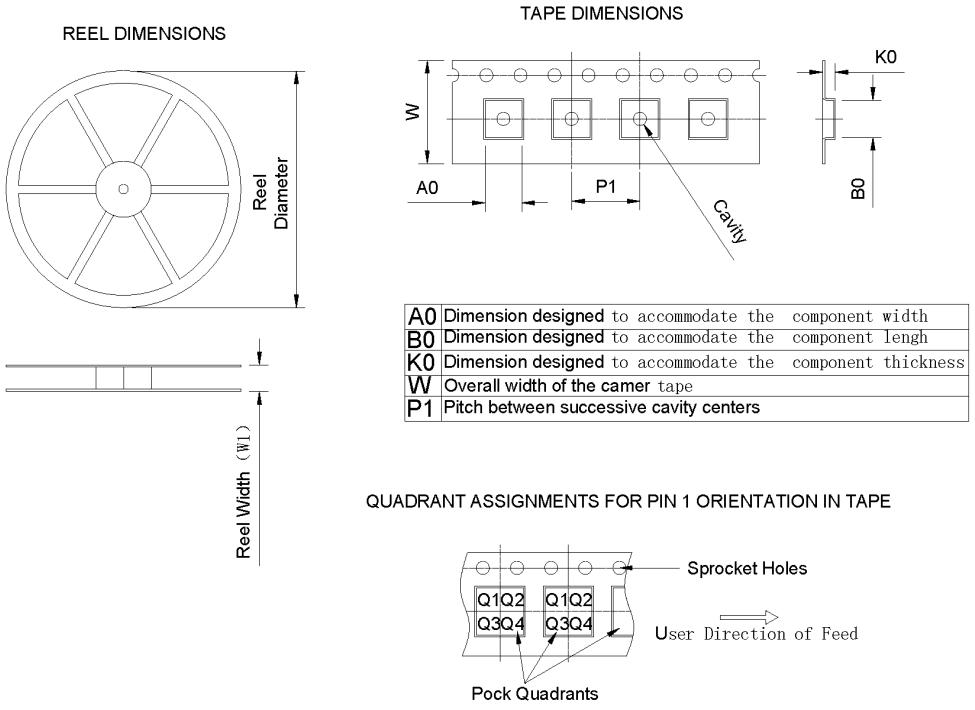


Figure 4. Package information

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
ARTC-4040-LP-PF	SOP8	8	3000	330±1	12.4±0.2	6.40	5.30	2.10	8.00±0.1	12.00±0.1	Q1
ARTC-4040-LPT-PF	TSSOP8	8	3000	330±1	12.4±0.2	5.3±0.1	3.3±0.1	1.25±0.1	8.00±0.1	12.00±0.1	Q1

Drawing control: (Internal use only)
Commodity code: TBD
Issue number : N1
Date : 16/06/2026
Internal reference : D1