ARTC-1010-LPHA-PF —Low Power Consumption High Accuracy I²C RTC

Key Features

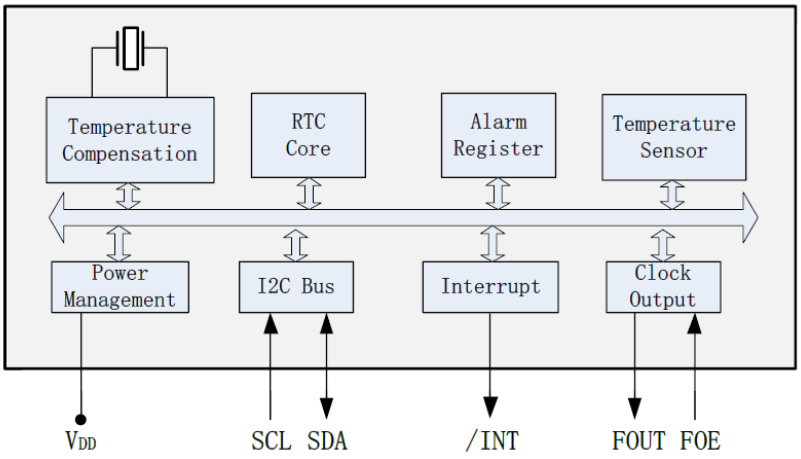
- Low current consumption: 1.0uA (Typ.)
- High stability:

  ±3.4ppm @ -40℃ ~ +85℃
- Build-in TCXO: 32.768KHz
- Build-in temperature sensor
- Communication Interface: I²C bus
- Power Supply Voltage: 1.6V~5.5V
- Operation Temperature Range: -40℃ ~ +85℃
- Leap years autocorrection
- Timer output function with adjustable period
- Package: 10.1mm × 7.4mm × 3.2mm (SOP14)
- RoHS & REACH compliant

Ordering Information

Part Name	Manufacture Part Number (MPN)	Description
ARTC-1010-LPHA-PF	ARTC-1010-LPHA-PF-PF	±3.4ppm@-40℃~+85℃

Block Diagram



Overview

The ARTC-1010-LPHA-PF is a high-accuracy I²C bus interface real-time clock with low power consumption. It embeds a 32.768KHz TCXO. The highly precise temperature sensor and temperature compensated circuit ensure high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. These features make it very suitable for energy, power devices and high-speed railway system applications.

1 Overview

The ARTC-1010-LPHA-PF is a high-accuracy I²C bus interface real-time clock with a low power consumption. It implements a 32.768KHz TCXO. The highly precise temperature sensor and temperature compensated circuit ensure high clock accuracy. It supports calendar (year, month, day, hour, minute, second), clock and timer functions etc. These features make it very suitable for energy, power devices and high-speed railway system applications.

2 Block Diagram

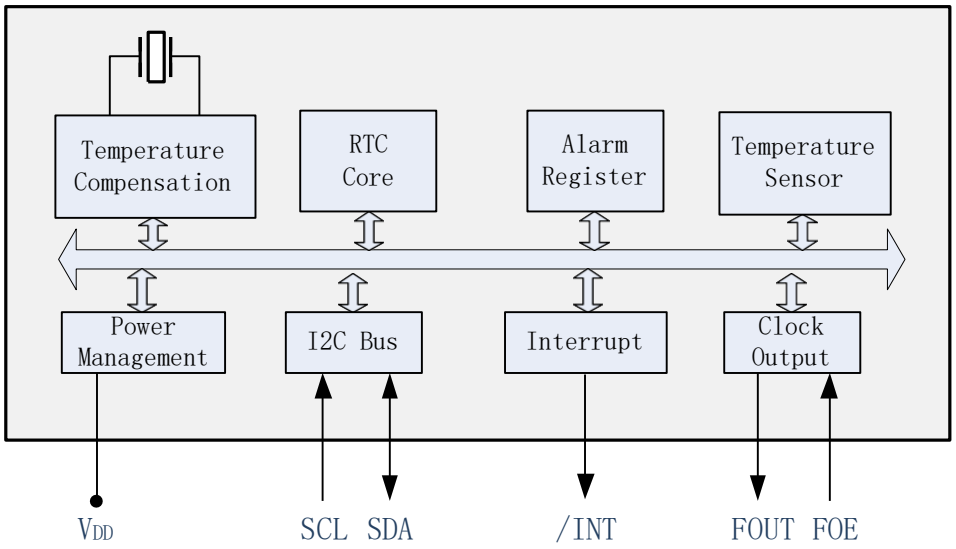


Figure 1. Block Diagram

3 Features

- Low current consumption: 1.0uA (Typ.)
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  ±3.4ppm @ -40℃ ~ +85℃
- Communication Interface: I2C bus
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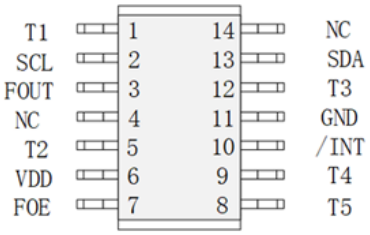
4 Pin definition

Table1. Pin Definition



Pin Number	Pin Name	I/O	Description
1	T1	-	Manufacturer test only. Must be floating.
2	SCL	In	I²C clock signal
3	FOUT	Out	Frequency output. Controlled by FOE. Frequency can be set by FSEL bits.
5	T2	-	Manufacturer test only. Must be floating.
6	V_{DD}	-	Power supply
7	FOE	In	FOUT output control pin. “1” - enable FOUT, “0”- FOUT Hi-Z
8	T5	-	Manufacturer test only. Must be floating.
9	T4	-	Manufacturer test only. Must be floating.
10	/INT	Out	Interrupt Output, Open-Drain
11	GND	-	Ground
12	T3	-	Manufacturer test only. Must be floating.
13	SDA	In/Out	I²C data signal
4, 14	NC	-	Leave to be floated or connected to VDD or GND

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table2. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-0.3		6.5	V	
Input Voltage	V_{IN}	GND-0.3		6.5	V	FOE, SCL, SDA input
Clock Output Voltage	V_{OUT1}	GND-0.3		V_{DD}+0.3	V	FOUT output
Output Voltage	V_{OUT2}	GND-0.3		6.5	V	SDA, /INT output
Storage temperature	T_{STG}	-55		125	℃	

5.2 Recommended Operating Conditions

Table3. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	1.6	3.0	5.5	V	
Operation temperature	T_{OPR}	-40	25	85	℃	

Note 1: V_{DD} needs to be at least 2.5V for the oscillation to stabilize (oscillation start time t_{STA}).

Note2：After power off, ensure that V_{DD}=GND for more than 10 seconds before next power on.

Note3：If there is no special indication, the test conditions are GND = 0V, VDD = 2.5V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.3 Frequency Characteristics

Table4. Frequency Characteristics

Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Frequency stability	Δf/f	-3.4		+3.4	ppm	-40℃ ~ +85℃
Oscillation start time	t_{STA}			1	s	@25℃
Year Aging	f_a			±3	ppm	@25℃, First year
Temperature Sensor Accuracy	T_{emp}			±5	℃	V_{DD}=3.0V
FOUT duty cycle	$t_{w/t}$	40	50	60	%	

Note：If there is no special indication, the test conditions are GND = 0V, VDD = 2.5V ~ 5.5V, Ta = - 40 ℃ ~ + 85 ℃

5.4 DC Characteristics

Table5. DC Characteristics

Parameter	Symbol	Value			Unit	Notes	
		Min.	Typ.	Max.			
Average Current consumption1	I_{DD1}		1.25	5.1	uA	V_{DD}=5.0V	f_{SCL}=0Hz, FOE=GND, /INT = V_{DD};; FOUT off (High-Z); Compensation interval 2s;
Average Current consumption2	I_{DD2}		1.0	4.9		V_{DD}=3.0V	
Average Current consumption3	I_{DD3}		5.8	20	uA	V_{DD}=5.0V	f_{SCL}=0Hz, FOE=V_{DD}, /INT = V_{DD}; FOUT:32.768kHz, CL=0pF; Compensation interval 2s;
Average Current consumption4	I_{DD4}		3.8	19		V_{DD}=3.0V	
High-level input voltage	V_{IH}	0.8*V_{DD}		5.5V	V	SCL, SDA, FOE pin	
Low-level input voltage	V_{IL}	GND-0.3		0.2*V_{DD}	V		
High-level output voltage	V_{OH1}	4.0		5.0	V	V_{DD}=5.0V, I_{OH} = -1mA	FOUT pin
	V_{OH2}	2.2		3.0		V_{DD}=3.0V, I_{OH} = -1mA	
	V_{OH3}	2.9		3.0		V_{DD}=3.0V, I_{OH} = -100uA	
Low-level output voltage	V_{OL1}	GND		GND+0.5	V	V_{DD}=5.0V, I_{OL} = 1mA	FOUT pin
	V_{OL2}	GND		GND+0.8		V_{DD}=3.0V, I_{OL} = 1mA	
	V_{OL3}	GND		GND+0.1		V_{DD}=3.0V, I_{OL} = 100uA	
	V_{OL4}	GND		GND+0.25	V	V_{DD}=5.0V, I_{OL} = 1mA	/INT pin
	V_{OL5}	GND		GND+0.4		V_{DD}=3.0V, I_{OL} = 1mA	
	V_{OL6}	GND		GND+0.4	V	V_{DD}≥3.0V, I_{OL} = 3mA	SDA pin
Input leakage current	I_{LK}	-0.5		0.5	uA	FOE, SDA, SCL pin, V_{IN} = V_{DD} or GND	
Output leakage current	I_{OZ}	-0.5		0.5	uA	FOUT, SDA, /INT pin, V_{IN} = V_{DD} or GND	

Note：If there is no special indication, the test conditions are GND = 0V, VDD = 2.5V ~ 5.5V, Ta = -40 ℃ ~ + 85 ℃

5.5 AC Characteristics

Table 6. AC Characteristics

V_{DD}=2.5V ~ 5.5V; Ta=-40℃ ~ +85℃

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}			400	kHz
SCL low level time	t_{LOW}	1.3			us
SCL high level time	t_{HIGH}	0.6			us
Start condition setup time	$t_{HD;STA}$	0.6			us
Start condition hold time	$t_{SU;STA}$	0.6			us
Stop condition setup time	$t_{SU;STO}$	0.6			us
Bus idle time between start condition and stop condition	t_{RCV}	1.3			us
Data setup time	$t_{SU;DAT}$	100			ns
Data hold time	$t_{HD;DAT}$	0		0.9	us
SCL, SDA rising time	t_r			0.3	us
SCL, SDA falling time	t_f			0.3	us

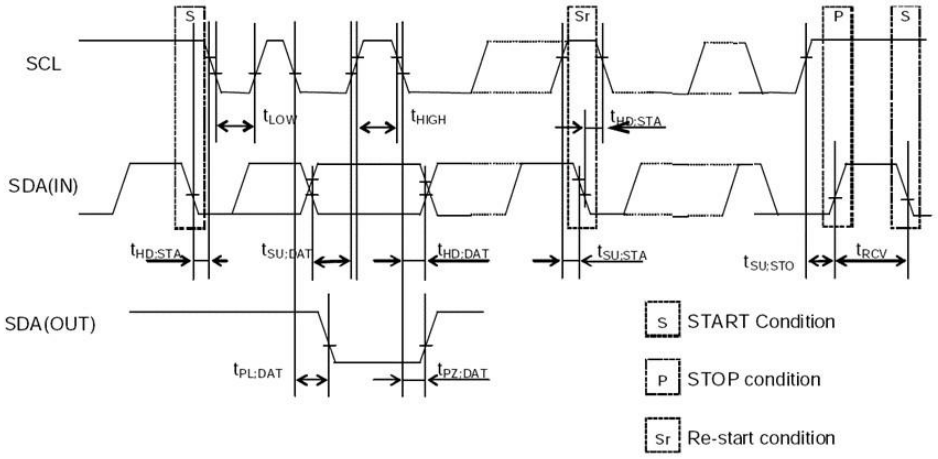


Figure 2. I²C bus Timing Chart

Note: When the master accesses the equipment through the I2C bus, all communication from the sending start condition to sending stop shall be completed within 1 second. If it exceeds 1 second, the I2C bus interface will be reset through the internal bus timeout function.

6 Registers

6.1 Register Lists

Address 0x00~0x0F: Basic Time and Calendar Registers

Address 0x10~0x1F: Extended Register Group 1

Address 0x20~30: Extended Register Group 2

Note: 0x10~16 and 0x00~06 with the same function, 0x1B~1F and 0x0B~0F with the same function

Table7. Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x00	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x01	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x02	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x03	WEEK	○	6	5	4	3	2	1	0	R/W
0x04	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x05	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x06	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x07	RAM	●	●	●	●	●	●	●	●	R/W
0x08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x09	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x0B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x0C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x0D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0x0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0x0F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	R/W

Table8. Extended Register Group 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
0x11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
0x12	HOUR	○	○	BCD code, Hour tens		BCD code, Hour ones place, 0-9				R/W

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
				place, 0-2						
0x13	WEEK	○	6	5	4	3	2	1	0	R/W
0x14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0x15	MONTH	○	○	○	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
0x16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
0x17	TEMP	128	64	32	16	8	4	2	1	R
0x18	RSV	Reserved								R/W
0x19	Not use	○	○	○	○	○	○	○	○	R
0x1A	Not use	○	○	○	○	○	○	○	○	R
0x1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0x1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0x1D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0x1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0x1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	R/W

Table9. Extended Register Group2

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0x20	Device ID	Vendor ID[3:0]				Ver[3:0]				R
0x21	RSV	Reserved: Ensure to be 0x80								R/W
0x22-24	RSV	Reserved: Not use								R/W
0x25	Offset0	○	○	○	○	○	S[4:2]			R/W
0x26	Offset1	S[1:0]		D[5:0]						R/W
0x27	SubSEC	Reserved				SubSEC[3:0]				R
0x28-30	RSV	Reserved: Ensure to be 0x00								R/W

Note:

1. After power-up reset or in case VLF bit returns “1”, make sure to initialize all registers to their default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- ✓ During the initial power-up, the bits below will be in the state as noted below:

  Initial 0:TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET,
  Initial 1: VLF, VDET, CSEL[0].

- ✓ All other register values are undefined, so make sure to reset the module before using it.
- ✓ The bits marked with “○” can be read out “0” only after initializing.
- ✓ The bits marked with “●” are RAM bits which can be used to write or read any data.
- ✓ Only 0 can be written to UF, TF, AF, VLF, VDET bits.
- ✓ Make sure “0” to be written for TEST bits which are used for testing only.
- ✓ Reserved bits must be set to the defined values accordingly.

6.2 Details of Registers

6.2.1 Clock counter registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x00/10	SEC	○	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x00
0x01/11	MIN	○	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x02/12	HOUR	○	○	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x00

SEC: BCD format, Value: 0~59

MIN: BCD format, Value: 0~59

HOUR: BCD format, Value: 0~23

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x03/13	WEEK	○	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h. Only one bit can be set to 1 each time, all others must be set to 0.

Table10. WEEK Register

WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x04/14	DAY	○	○	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range will be adjusted automatically according to the month setting and if it is a leap year or not .

Table11. DAY Register Value

Month	Day Value Range
1, 3, 5, 7, 8, 10, 12	1~31
4, 6, 9, 11	1~30
February in normal year	1~28
February in leap year	1~29

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x05/15	MONTH	○	○	○	BCD code, Month	BCD code, Month ones place, 0-9				0x01

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
					tens place, 0-1					
0x06/16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value1~12

YEAR: BCD format, Value0~99(2000~2099)

Example: 2020/01/01 Wednesday 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00/10	SEC	○	0	1	1	0	1	1	0
0x01/11	MIN	○	0	0	1	1	0	0	0
0x02/12	HOUR	○	○	1	0	0	0	0	1
0x03/13	WEEK	○	0	0	0	1	0	0	0
0x04/14	DAY	○	○	0	0	0	0	0	1
0x05/15	MONTH	○	○	○	0	0	0	0	1
0x06/16	YEAR	0	0	1	0	0	0	0	0

6.2.2 Alarm registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
0x09	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Minute ones place, 0-9				0x00
0x0A	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
	DAY Alarm		●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time matches the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

WEEK Alarm/DAY Alarm: Controlled by WADA bit in 0x0D register

AE: Alarm Enable bit, 0-enable; 1-disenable

AF: Defined in 0x0E register bit3

AIE: Defined in 0x0F register bit3

6.2.3 Timer control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0B/1B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0x0C/1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	0x00

According to TE, TF, TIE, TSEL[1:0] bits setting, a timer interrupt will be generated once the value counts down to 0 from the one set in the above registers.

TE: Defined in 0x0D register bit4

TF: Defined in 0x0E register bit4

TIE: Defined in 0x0F register bit4

TSEL[1:0]: Defined in 0x0D register bit1 and bit0

6.2.4 Extension registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0D/1D	Extension Register	TEST	WADA	USEL	TE	FSEL[1]	FSEL[0]	TSEL[1]	TSEL[0]	0x02

TEST: Test bit, must be set to "0"
WADA: Week Alarm/Day Alarm control bit, decide 0x0A register as DAY Alarm or WEEK Alarm. 0-WEEK alarm, 1-DAY alarm
USEL: Update Interrupt Select bit, 0-output interrupt once a second, 1-output interrupt once a minute
TE: Timer Enable bit, 0-disenable, 1-enable

FSEL[1], FSEL[0]: FOUT frequency setting:

FSEL[1]	FSEL[0]	FOUT Frequency
0	0	32.768KHz (Default)
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

TSEL[1], TSEL[0]: Timer countdown period(source clock) setting:

TSEL[1]	TSEL[0]	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

6.2.5 Flag registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0E/1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	0x03

UF: Update flag bit. When a time update interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.
TF: Timer Flag bit. When a fixed-cycle timer interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.
AF: Alarm Flag bit. When an alarm interrupt event occurs, it will be set to "1" and keeps "1" until a "0" is written to it.
VLF: Voltage Low Flag bit. When supply voltage is lower than 1.4V, it will be set to "1" and keeps "1" until a "0" is written to it.
VDET: Voltage Detection Flag bit. When supply voltage is lower than 2.1V, it will be set to "1" and keeps "1" until a "0" is written to it.

6.2.6 Control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x0F/1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	○	○	RESET	0x40

CSEL[1], CSEL[0]: Compensation interval Select 1, 0 bits, used to set temperature compensation interval.

CSEL[1]	CSEL[0]	Compensation interval
0	0	0.5s
0	1	2s(default)
1	0	10s
1	1	30s

UIE: Update Interrupt Enable bit. When UF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
TIE: Timer Interrupt Enable bit: When TF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
AIE: Alarm Interrupt Enable bit: When AF changes from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disenable (/INT keeps Hi-Z), 1-enable (/INT status changes from Hi-Z to Low).
RESET: Reset IC, prepared for the synchronized starting of time or timer.

6.2.7 Temperature register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x17	TEMP	128	64	32	16	8	4	2	1	0x00

Read digital temperature data, Temp [°C] = (TEMP[7:0] * 2 -147.5) / 3.0448.

6.2.8 Device ID register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x20	Device ID	VendorID[3:0]				Ver[3:0]				0xD2

VendorID[3:0]: The fixed value is defined as VendorID[3:0]=1101b=Dh to represent ACT.
Ver[3:0]: version of the IC

6.2.9 RSV register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x21	RSV	Reserved: must be 0x80								0x80
0x22~ 0x24	RSV	Reserved: Not use								0x00

6.2.10 Frequency Offset register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x25	Frequency Offset0	Reserved	Reserved	Reserved	Reserved	Reserved	S [4]	S [3]	S [2]	0x00
0x26	Frequency Offset1	S [1]	S [0]	D [5]	D [4]	D [3]	D [2]	D [1]	D [0]	0x00

S [4:0]: Sign bits. Only 2b' 0 0000 and 2b' 1 1111 is legitimate.

D [5:0]: Data bits

S [4:0]	D [5:0]	Frequency Adjustment (ppm)
2b' 0 0000	2b'00 0000	0 (Default)
	2b'00 0001	-0.1
	2b'00 0010	-0.2
	…	…
	2b'11 1110	-6.2
	2b'11 1111	-6.3
2b' 1 1111	2b'11 1111	+0.1
	2b'11 1110	+0.2
	…	…
	2b'00 0010	+6.2
	2b'00 0001	+6.3
Other's	Other's	Invalid value, must be avoided.

Note: *The Frequency offset register affects the frequency stability. Please be careful if you adjust it.

The offset function is effective for frequency adjustments at the normal temperature.

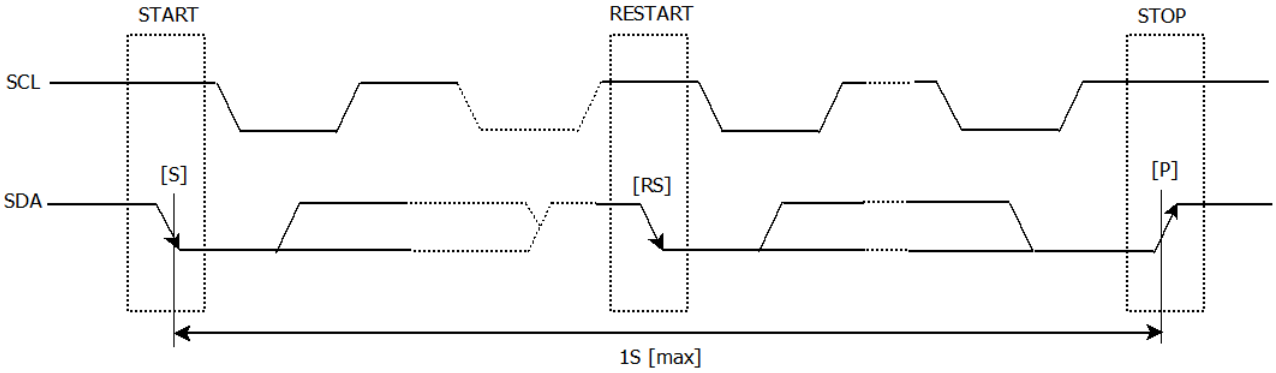
The single adjustment amount of 0.1ppm is the approximate value.

6.2.11 Sub-second timer register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x27	SubSEC	Reserved				SubSEC[3:0]				0x00

SubSEC[3:0]: sub second bit, and unit is 1/16s.

7 I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as "Master" and "Slave". ARTC-1010-LPHA-PF can only be used as Slave.

7.1 Cautions

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically. A new START condition must be transferred before restarting any communications.

ARTC-1010-LPHA-PF I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access. After 0xFF address, the next one will be 0x00.

7.2 Slave Address

Table12. I²C Bus Slave Address

Transfer data	Slave address							R/W
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
65h (Read)	0	1	1	0	0	1	0	1 (Read)
64h (Write)								0 (Write)

ARTC-1010-LPHA-PF I²C bus Slave Address is [0110 010*].

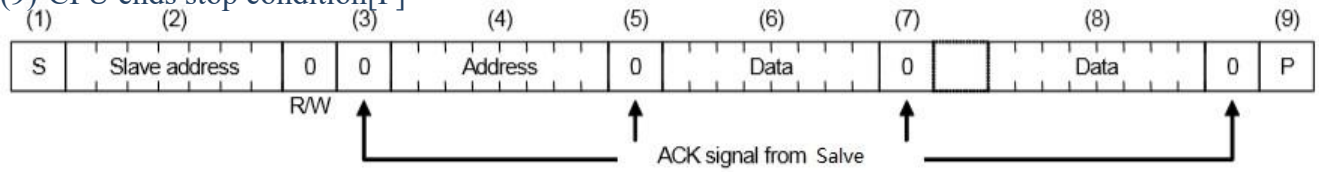
7.3 I²C bus protocol

It is assumed CPU is master and ARTC-1010-LPHA-PF is slave in this section.

7.3.1 Write process

I²C bus includes an address auto-increment function, once the initial address has been specified, the ARTC-1010-LPHA-PF increments (+1) the address automatically after each data is sent, then to write next data.

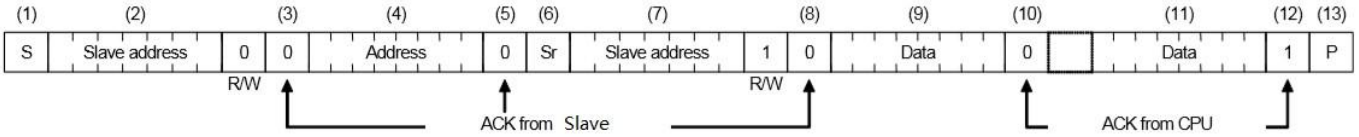
(1) CPU sends start condition[S]
(2) CPU sends ARTC-1010-LPHA-PF's slave address a R/W bit to set to write mode
(3) CPU verifies ACK signal from ARTC-1010-LPHA-PF
(4) CPU sends write address to ARTC-1010-LPHA-PF
(5) CPU verifies ACK signal from ARTC-1010-LPHA-PF
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from ARTC-1010-LPHA-PF
(8) Repeat (6) (7) if multiple bytes need to be written, address will be incremented automatically
(9) CPU ends stop condition[P]



7.3.2 Read process

Writing the address to be read with write mode first, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends ARTC-1010-LPHA-PF's slave address a R/W bit to set to write mode
(3) CPU verifies ACK signal from ARTC-1010-LPHA-PF
(4) CPU sends address for reading from ARTC-1010-LPHA-PF
(5) CPU verifies ACK signal from ARTC-1010-LPHA-PF
(6) CPU sends RESTART condition [Sr]
(7) CPU sends ARTC-1010-LPHA-PF's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from ARTC-1010-LPHA-PF
(9) CPU reads data from the specified address in step (4)
(10) CPU sends ACK signal for "0"
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]



8 Reflow Soldering Curve

Standard: IPC/JEDEC J-STD-020

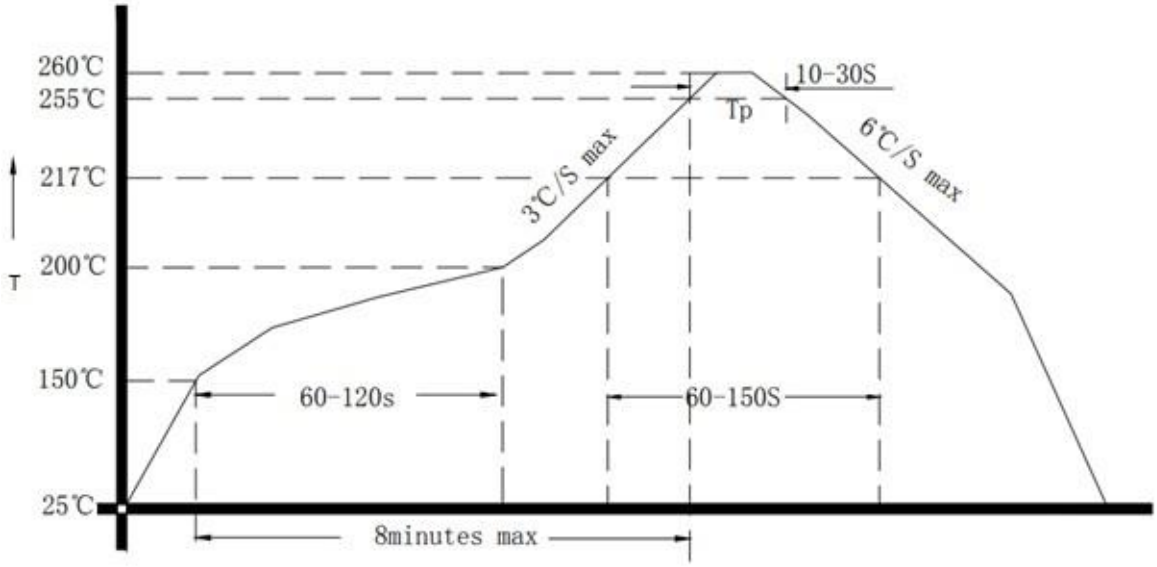
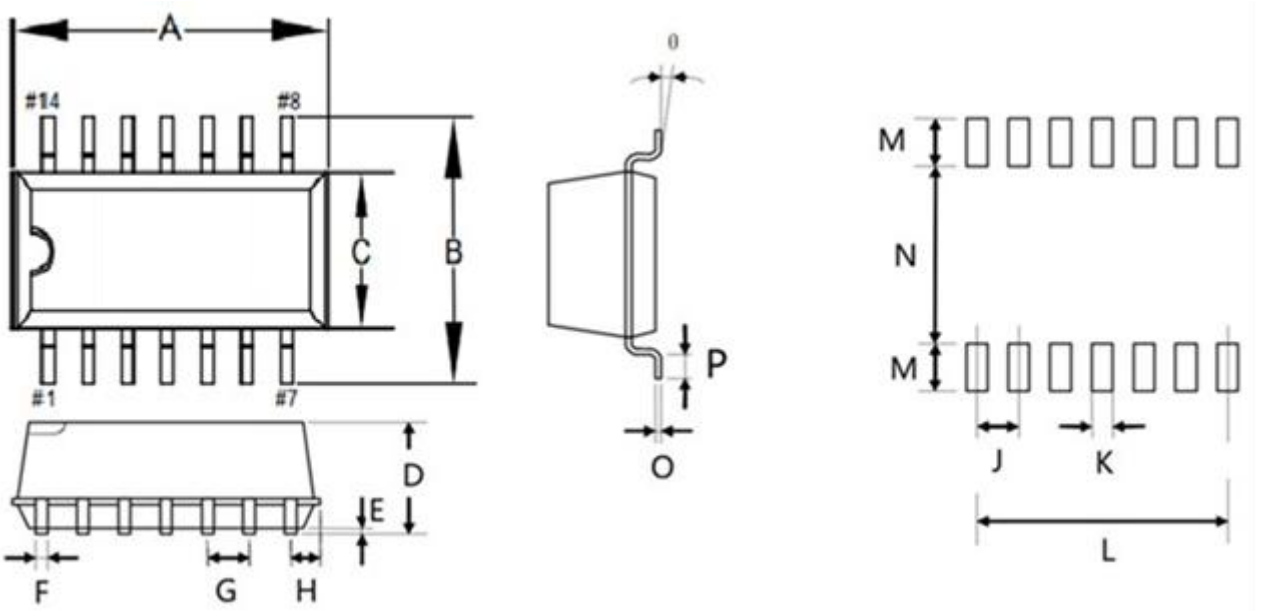


Figure 3. Reflow Soldering Curve

Note: It is suggested to solder IC under the conditions shown i n the curve above. You must pay attention to the temperature and time under heat when manual soldering. If the temperature is over +260℃ you will worsen the crystal performance or even damage it.

9 Package Dimensions



Dimension	Min.	Typ.	Max.
A	10.0	10.1	10.2
B	7.2	7.4	7.6
C	4.9	5.0	5.1
D	3.1	3.2	3.3
E	0.055	--	0.205
F	--	0.406	--
G	--	1.27	--
H	--	1.2	--
P	0.5	0.6	0.7
O	--	0.13	--
θ	1°		8°

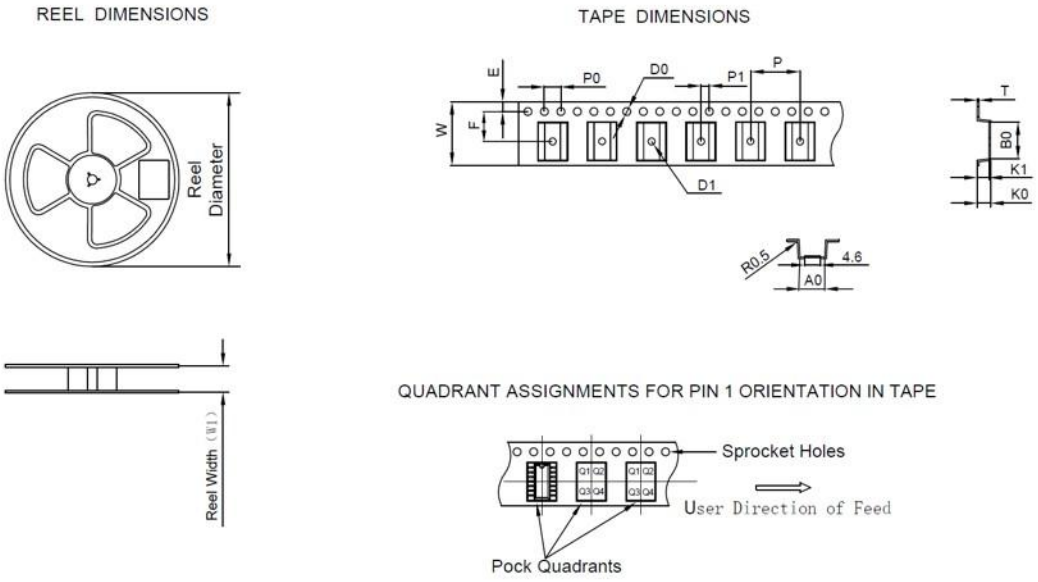
Unit : mm

Dimension	Typ.
J	1.27
K	0.7
L	7.62
M	1.4
N	5.4

Unit : mm

Figure 4. Recommended Soldering Pattern and Dimension

10 Packing Information



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	D0 (mm)	D1 (mm)	E (mm)	F (mm)	T (mm)	K0 (mm)	K1 (mm)	W (mm)	P (mm)	P0 (mm)	P1 (mm)	PIN1 Quadrant
ARTC-1010-LPHA-PF	SOP14	14	1300pcs	330	16	8.0 ± 0.1	10.4 ±0.1	1.5 ± 0.1	1.5 ± 0.1	1.75 ±0.1	7.5 ± 0.1	0.3± 0.05	3.8 ± 0.1	3.5 ± 0.1	16± 0.3	12± 0.1	4± 0.1	2± 0.1	Q1

Figure 5. Packing Information

Drawing control: (Internal use only)
Commodity code: TBD
Issue number : N1
Date : 10/06/2026
Internal reference : D1