ACB-3030-QFN-PF—2:4 Low Skew Clock Buffer

FEATURES

- Low skew outputs: 50ps(typ.)
- LVCMOS Output
- Operating Voltages of 1.8V/2.5V/3.3V
- Frequency input / output: 0~200MHz
- Output Enable pin tri-states outputs
- Lead-Free & RoHS Compliant
- Temperature range: -40°C to +85°C
- Packaged: QFN14L(2*2*0.55mm)

APPLICATIONS

- Wireless BBU, RRU and Wired Communication
- Switches, Routers, Line Cards, Timing Cards

GENERAL DESCRIPTION

The ACB-3030-QFN-PF is a low skew, dual input to four output, clock buffer. Perfect for fanning out multiple clock outputs. The input clock is distributed to four LVCMOS outputs which can be enabled or disabled by an OE pin. The ACB-3030-QFN-PF operates from a 1.8V/2.5V/3.3V power supply.

1 FUNCTIONAL BLOCK DIAGRAM

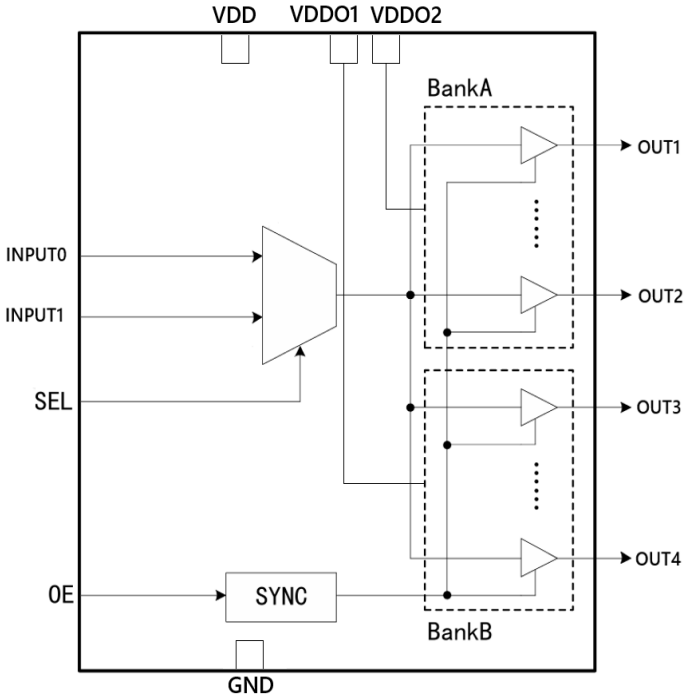


Figure 1. Block Diagram

2 PIN DESCRIPTION

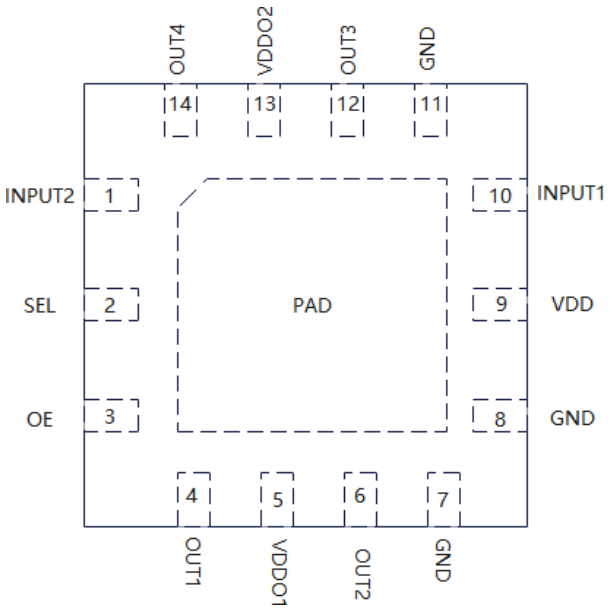


Figure 2. Pinouts Diagram

Table 1. Pin Definition

PIN No.	PIN Name	TYPE	DESCRIPTIONS
1	INPUT2	IN	Clock Input2.
2	SEL	IN	Clock input select pin. “L”: INPUT1 is enable “H”: INPUT2 is enable
3	OE	IN	Clock output control pin. “L”: Disable OUT1/2/3/4 “H”: Enable OUT1/2/3/4
4	OUT1	OUT	Clock output 1
5	VDDO1	PWR	Power supply for OUT1/2 (BANKA)
6	OUT2	OUT	Clock output 2
7	GND	-	GND
8	GND	-	GND
9	VDD	PWR	Power supply for VCORE
10	INPUT1	IN	Clock Input1.
11	GND	-	GND
12	OUT3	OUT	Clock output 3
13	VDDO2	PWR	Power supply for OUT3/4 (BANKB)
14	OUT4	OUT	Clock output 4
15	PAD	-	GND

3 ELECTRICAL CHARACTERISTICS

Table 2. Absolute Maximum Ratings

Stresses beyond those listed under the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for extended periods may affect product reliability.

Parameter	Symbol	Rating	Unit
Power Supply	V_{DD}	-0.5～4.6	V
Input Voltage	V_{IN}	-0.5～V_{DD}+0.5	V
Output Voltage	V_{OUT}	-0.5～V_{DD}+0.5	V
Storage Temperature Range	T_{STG}	-65～150	℃
Maximum Junction Temperature	T_J	150	℃
Thermal Impedance	θ_{JA}	123	℃/W

Table 3. Recommended Operating Conditions

Test Condition: -40℃≤T_A≤85℃; It is recommended that the chip operates within the rated electrical range indicated in the table below.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
Power Supply	V_{DD}	3.135	3.3	3.465	V	
		2.375	2.5	2.625		
		1.71	1.8	1.89		
	$V_{DDO1/2}$	1.71		3.465		$V_{DDO1/2}$ must smaller than V_{DD}
Static Device Current	I_{VDD}		23		mA	V_{DD}=3.3V, F_{OUT}=26MHz T_A=85℃
Power dissipation capacitance per output	C_{PD}		9		pF	V_{DD} =3.3V, F_{OUT}=26MHz
Operating Temperature Range	T_A	-40		85	℃	

Table 4. Control Signal Characteristics

Test Condition：-40℃≤T_A≤85℃, 1.71V≤V_{DD}≤3.465V, $F_{IN/OUT}$=26MHz; Unless otherwise noted.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Control Signal (OE)						
Input High Current	I_{IH}			40	uA	

Input Low Current	I_{IL}	-40			uA	
Input High Voltage	V_{IH}	0.7*V_{DD}			V	V_{DD} =3.3V
Input Low Voltage	V_{IL}			0.3*V_{DD}	V	V_{DD} =3.3V

Table 5. INPUT Characteristics

Test Condition：-40℃≤TA≤85℃, 1.71V≤V_{DD}≤3.465V, Unless otherwise noted.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Frequency	F_{INPUT}	0		200	MHz	
Input High Voltage	V_{INPUTH}	0.7*V_{DD}		V_{DD}+0.3	V	
Input Low Voltage	V_{INPUTL}	-0.3		0.3*V_{DD}	V	

Table 6. Output Characteristics

Test Condition：-40℃≤T_A≤85℃, 1.71V≤V_{DD}≤3.465V, 1.71V≤$VDDO_X$≤3.465V, $F_{IN/OUT}$=26MHz, C_L=5pF//50Ω; Unless otherwise noted.

Parameter	Symbol	Value			Unit	Comments
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	0.8*V_{DD}			V	V_{DD}=1.71～ 3.465V
Output High Voltage	V_{OL}			0.2*V_{DD}	V	V_{DDOX}=1.71～3.465V
Output impedance	R_O	15		30	Ω	
Output Frequency	F_{OUT}	0		200	MHz	
Duty Cycle	Duty Cycle	40	50	60	%	
Output Skew	$t_{Skew(*)}$	30	50	80	ps	
Part-to-part skew	$t_{PDP(*)}$			2	ns	

Output Delay	t_{Delay}		4.0	5.0	6.0	ns	V_{DD}=3.3V/2.5V
			6.0	7.0	9.0	ns	V_{DD}=1.8V
Rise/Fall Time	t_{Rise} / t_{Fall}				10	ns	V_{DD}=3.3V/2.5V/1.8V CL=5pF//50ohm Output=26MHz
ADD Phase Noise	PN	1kHz offset		-146.0		dBc/Hz	F_{OUT}=20MHz CL=5pF 12kHzto10MHz Input sight Jitter=146(fs)
		10kHz offset		-155.0			
		100kHz offset		-160.0			
		1MHz offset		-164.0			
		5MHz offset		-165.4			
Additive RMS Phase Jitter（RMS）	t_J			220		fs	V_{DD}=3.3V V_{DDOX}=3.3V F_{OUT}=20MHz CL=5pF 12kHzto10MHz Input sight Jitter=146(fs)
Output enable time	t_{EN}			90		ns	V_{DD}=3.3V CL=5pF RL=50ohm
Output disable time	t_{dis}			1.5		us	V_{DD}=3.3V CL=5pF RL=50ohm

* Parameter is specified by design, not tested in production

4 FUNCTION DESCRIPTION

4.1 Control Signals

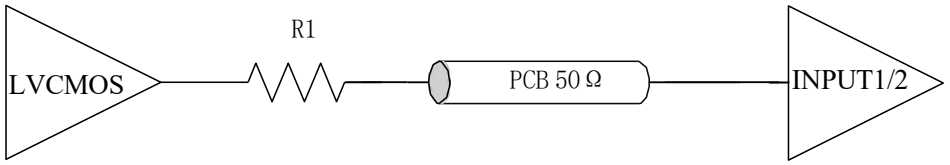
The outputs provide 4 LVCMOS copies of the input clock. The LVCMOS output high level is referenced to the V_{DD} voltage. The outputs can be enabled or disabled using the enable input pin, OE, as shown in Table 7.

Table 7. Reference Output Enable

OE	Outputs State
0	Hi-Z
1	Enabled

4.2 Input Clock

The INPUT could be a LVCMOS clock as shown in Figure 3. It is better to route the clock trace on the component side with a serial resistor close to the output pin (<=200mil).

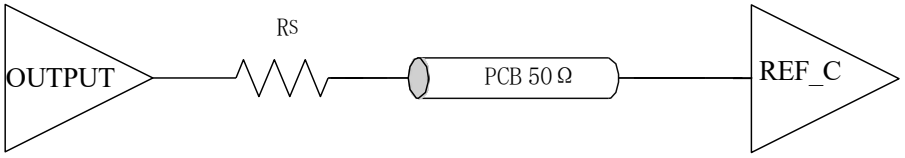


R1: Source end matching Resistor

Figure 3. LVCMOS Input Clock

4.3 CLOCK OUTPUTS

The ACB-2020-LS-PF has 4 LVCMOS outputs OUT1, OUT2, OUT3, OUT4. A serial terminating resistor may be used on each clock output if the trace is longer than 1 inch.



R_S: Source end matching Resistor
R_O: Output impendence
$R_S+R_O=50\Omega$

Notes

- Unused outputs could be left floating to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

4.4 Power Supply

V_{DD} is ACB-2020-LS-PF power supply voltage support 1.8V/2.5V/3.3V.

Notes

- .1uF or 0.01uF bypass capacitors should be placed very close to each supply pin
- 1uF to 10uF Decoupling capacitors should be placed nearby

5 ENVIRONMENT

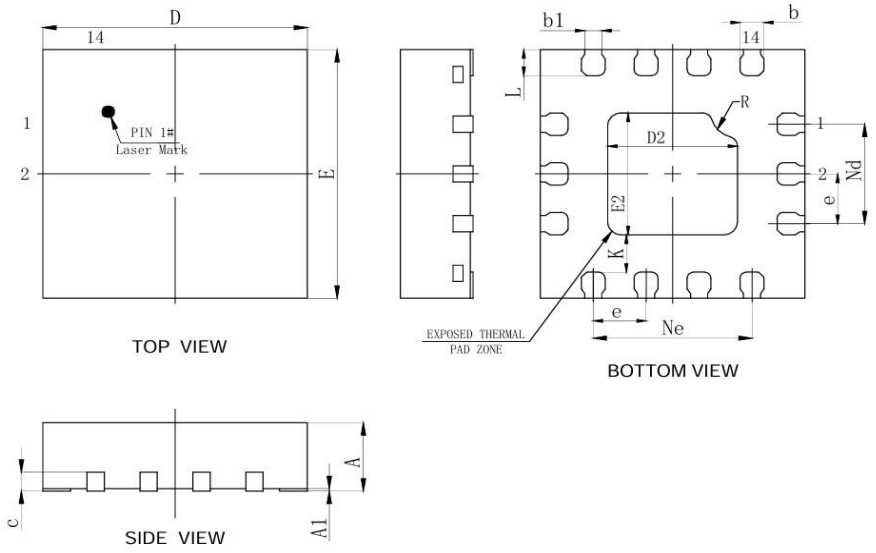
Table 9. ENVIRONMENT CONDITIONS

Parameters	Value	Unit	Notes
ESD Level	±2000V	V	HBM, Refer to ANSI/ESDA/JEDEC JS-001-2010
	±800V	V	CDM, Refer to JEDEC specification JESD22-C101

* HBM： Human body model

CDM： Charged-device model

6 PACKAGE OUTLINE



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1	0.13REF		
c	0.152REF		
D	1.90	2.00	2.10
D2	0.88	0.98	1.08
e	0.40BSC		
Ne	1.20BSC		
Nd	0.80BSC		
E	1.90	2.00	2.10
E2	0.88	0.98	1.08
L	0.16	0.21	0.26
R	0.20REF		
K	0.25	0.30	0.35

Figure 5. Package Outline Diagram

Drawing control: (Internal use only)
Commodity code: TBD
Issue number : N1
Date : 11/06/2026
Internal reference : D1