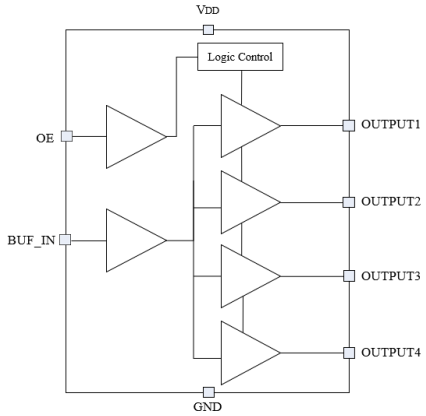
ACB-2020-LS-PF

1:4 Low Skew Clock Buffer, SOIC-8, 8 pin

Features:

- Low skew outputs (50ps)
- Low power CMOS technology
- Operating Voltages of 3.3V/2.5V ± 5%
- Output Enable pin tri-states outputs
- 3.6 V tolerant input clock
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free. “Green” Device
- Industrial temperature range: -40°C to +85°C
- Packaged: 8-pin SOIC



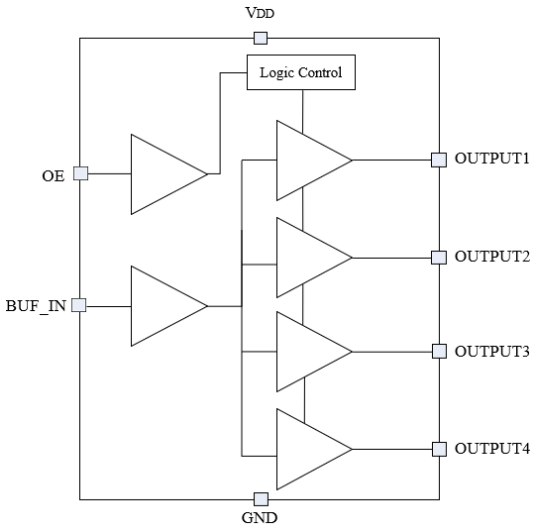
Applications:

- Wireless BBU, RRU and Wired Communication
- Servers, Computing, PCI Express (PCIe)
- Switches, Routers, Line Cards, Timing Cards

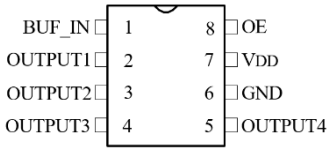
Product Overview

The ACB-2020-LS-PF is a low-skew, single input to four output clock buffers. Perfect for fanning out multiple clock outputs. The input clock is distributed to four LVCMOS outputs which can be enabled or disabled by OE pin. The ACB-2020-LS-PF operates from a 3.3V/2.5V power supply.

Block Diagram



Pinout



I/O

Pin	Name	I/O	Description
1	BUF_IN	I	Clock Input. 3.3 V tolerant input.
2	OUTPUT1	O	Clock output 1
3	OUTPUT2	O	Clock output 2
4	OUTPUT3	O	Clock output 3
5	OUTPUT4	O	Clock output 4
6	GND	GND	Ground
7	V_{DD}	PWR	2.5V or 3.3V
8	OE(Output Enable)	I	Tri-states outputs when low. Connect to VDD for normal operation.

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Electrical Characteristics

Absolute Maximum Ratings				
Parameter	**Symbol**	**Rating**	**Unit**	**Notes**
Power Supply	V_{DD}	-0.5～4.6	V	
Input Voltage	V_{IN}	-0.5～VDD+0.5	V	
Output Voltage	V_{OUT}	-0.5～VDD+0.5	V	
Storage Temperature Range	T_{STG}	-65～150	℃	
Maximum Junction Temperature	T_J	150	℃	
Thermal Impedance	Θ_{JA}	123	℃/W	

Note: Stresses beyond the parameters listed under absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for extended periods may affect product reliability.

Test conditions: -40℃≤TA≤85℃. It is recommended to operate the chip within the rated electrical ranges specified below.

Recommended Operating Conditions				
Parameter	**Symbol**	**Rating**	**Unit**	**Notes**
Power Supply	V_{DD}	3.315～3.465	V	3.3V Typ.
		2.375～2.625	V	2.5V Typ.
Static Device Current	I_{VDD}	20	mA	V_{DD} = 3.3V
Power dissipation capacitance per output	C_{PD}	9	pF	V_{DD} = 3.3V, F_{OUT} = 100MHz
Operating temperature range	T_A	-40～-85	℃	

Test Conditions：-40℃≤TA≤85℃, 2.375V≤VDD≤3.465V, Unless otherwise noted.

Control Signal Characteristics						
Parameter	**Symbol**	**Rating**			**Unit**	**Notes**
		Min.	**Typ.**	**Max.**		
Control Signal (OE)						
Input High Current	I_{IH}			40	uA	
Input Low Current	I_{IL}	-40			uA	
Input High Voltage	V_{IH}	0.7*V_{DD}			V	
Input Low Voltage	V_{IL}			0.3*V_{DD}	V	

Test Condition：-40℃≤TA≤85℃, 2.375V≤VDD≤3.465V, Unless otherwise noted.

BUF_IN Characteristics						
Parameter	**Symbol**	**Rating**			**Unit**	**Notes**
		Min.	**Typ.**	**Max.**		
Frequency	F_{BUF_IN}			100	MHZ	
Input High Voltage	V_{BUF_INH}	0.7*V_{DD}		V_{DD}+0.3	V	
Input Low Voltage	V_{BUF_INL}	-0.3		0.3*V_{DD}	V	

Test Condition：-40℃≤TA≤85℃, 2.375V≤VDD≤3.465V, FIN/OUT=100MHz, CL=5pF//50Ω; Unless otherwise noted

Output Characteristics						
Parameter	**Symbol**	**Rating**			**Unit**	**Notes**
		Min.	**Typ.**	**Max.**		
Output High Voltage	V_{OH}	0.8*V_{DD}			C	V_{DD}=2.375～3.465V
Output Low Voltage	V_{OL}			0.2*V_{DD}	V	V_{DDOX}=2.375～3.465V
Output impedance	R_O		15		Ω	V_{DD}=3.3V
			20		Ω	V_{DD}=2.5V
Output Frequency	F_{OUT}	0		100	MHz	
Duty Cycle	Duty Cycle	45	50	55	%	
Output Skew	t_{skew}*		30	50	ps	
Part-to-part skew	t_{PDP}*			2		

Output delay	T_{Delay}	1.5	1.95	4.0	ns	V_{DD}=3.3V
		1.8	2.4	4.4	ns	V_{DD}=2.5V
Rise/Fall Time	t_{Rise}/t_{Fall}		3.0		ns	V_{DD}=3.3V CL=15pF
			4.4		ns	V_{DD}=3.3V CL=50pF
			5.0		ns	V_{DD}=3.3V CL=100pF
Additive RMS Phase Jitter （RMS）	t_J		50		fs	F_{OUT}=25MHz Input skew rate ≥2V/ns CL=5pF 12kHz to 20MHz
Output enable or disable time	t_{EN}			2	Cycles	

*Parameter is specified by design, not tested in production

Function Description

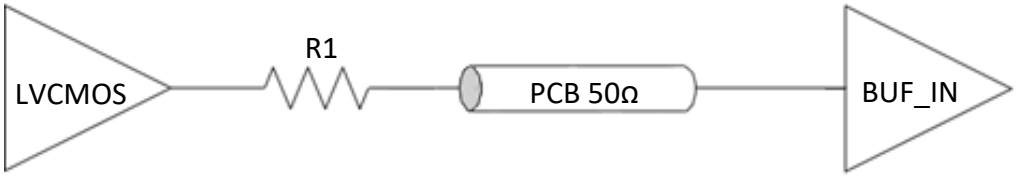
Control Signals

The outputs provide 4 LVCMOS copies of the input clock. The LVCMOS output high level is referenced to the VDD voltage. The outputs can be enabled or disabled using the enable input pin, OE, as shown in the table below.

OE	Output State
0	Hi – Z
1	Enabled

Input Clock

The BUF_IN input could be a LVCMOS input clock up to 100MHz as in the figure below. It is better to route the clock trace on the component side with a series resistor close to the output pin (<=200mil).

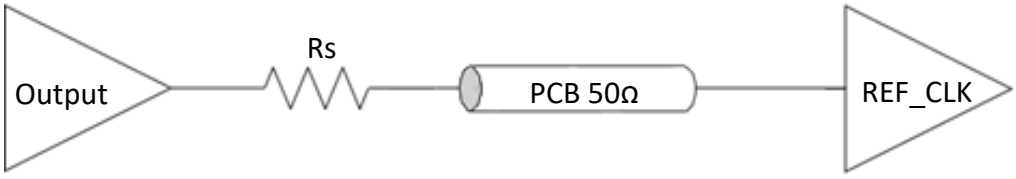


R1 :Source end matching Resistor

LVCMOS Input Clock

Output Clock

The ACB-2020-LS-PF has 4 LVCMOS outputs OUTPUT1, OUTPUT2, OUTPUT3, OUTPUT4. A serial terminating resistor may be used for each clock output if the trace is longer than 1 inch.



Rs :Source end matching Resistor
Rs + R0 = 50Ω

Output Termination

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Input vs Output States	
Input Clock	Output State
BUF_IN = Logic High	Logic High
BUF_IN = Logic Low	Logic Low

Notes:
Unused outputs could be left floating to minimize capacitance. Yhis way, this output will consume minimal output current because it has no load.

Power supply

The ACB-2020-LS-PF supports both 3.3V and 2.5V V_{DD} power supply voltage.

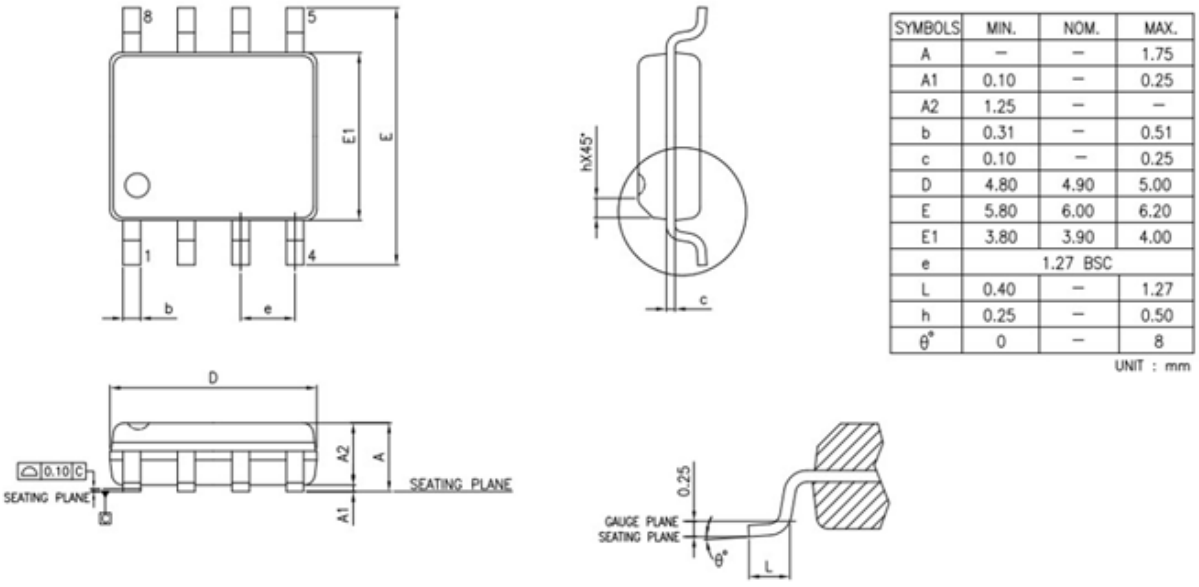
Notes:
.1uF or 0.01uF bypass capacitors should be placed very close to each supply pin
1uF to 10uF Decoupling capacitors should be placed nearby

Environmental Specifications

Parameters	Value	Unit	Notes
ESD Level	±2000V	V	HBM, Refer to ANSI/ESDA/JEDEC JS-001-2010
	±800V	V	CDM, Refer to JEDEC specification JESD22-C101

Notes:
HBM： Human body model
CDM： Charged-device model

Dimensions (mm)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

UNIT : mm

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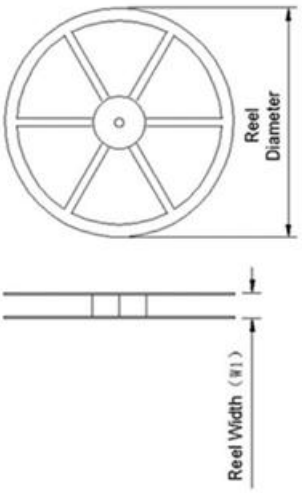
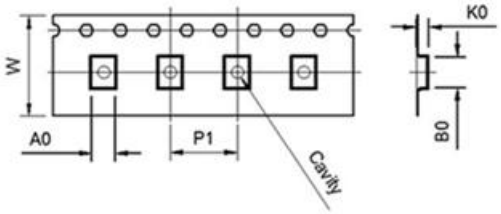
Tape and Reel Specification

REEL DIMENSIONS

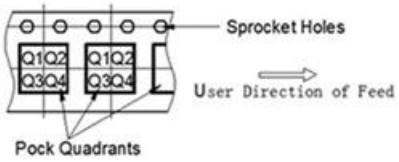


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 Quadrant
ACB-2020-LS-PF	SOP	8	3000	330±1	12.4±2	6.4	5.3	2.1	8.0±0.1	12.0±0.1	Q1

Drawing control: (Internal use only)
Commodity code: TBD
Issue number : N1
Date : 10/06/2026
Internal reference : D1