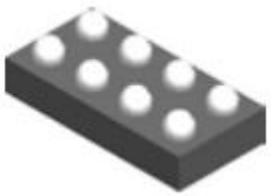
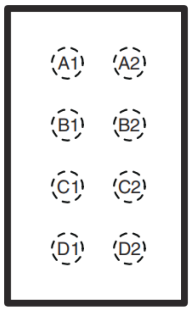
ACTINS6102B-PF

Low-Jitter Clock Buffer, WLCSP (0.8mm × 1.6mm), 8 pin, YFP 0.4mm

Features:

- Support 2 LVCMOS Output (10MHz～80MHz)
- Sine wave and square wave input
- Minimum sine wave of 0.3V signal (peak to peak)
- Internal integrated AC coupling
- Low additional phase jitter
- LVCMOS Input：0.35ps（fIN = 26 MHz， Vpp = 0.8V， BW=10Hz~5MHz）
- Square Wave Input：0.40ps（fIN = 26 MHz， Vpp = 1.4V， BW=10Hz~5MHz）
- 1.8V LDO Output
- Level shift function for high and low output voltage
- Package: WLCSP (0.8mm × 1.6mm), 8 pin, YFP 0.4mm
- Operating Temperature：-40℃ ～ +85℃
- RoHS compliant





Applications:

- Mobile
- GPS
- Wireless LAN
- FM radio
- WiMAX
- W-BT

Description:

The ACTINS6102B-PF is a dual-channel clock fan-out buffer designed for portable terminal devices such as mobile phones that require clock buffering with low additional phase noise and fan-out capability. This device buffers a single master clock, such as a temperature-compensated crystal oscillator (TCXO), to multiple peripherals. The device supports two clock request inputs (CLK_REQ1 and CLK_REQ2), each of which supports a single clock output, and the6102B also supports high/low level shift functionality.

Product Overview

The ACTINS6102B-PF is a dual-channel clock output driver circuit featuring clock driving capability, minimal additional phase noise, and extremely small inter-channel skew. It is suitable for portable terminal devices (such as mobile phones) that require clock buffering with minimal additional phase noise and fan-out functionality. The chip drives and outputs clock signals from sources like temperature-compensated crystal oscillators (TCXOs) to multiple peripherals. It supports two clock request inputs, CLK_REQ1 and CLK_REQ2, with each output individually enabled by its corresponding request signal.

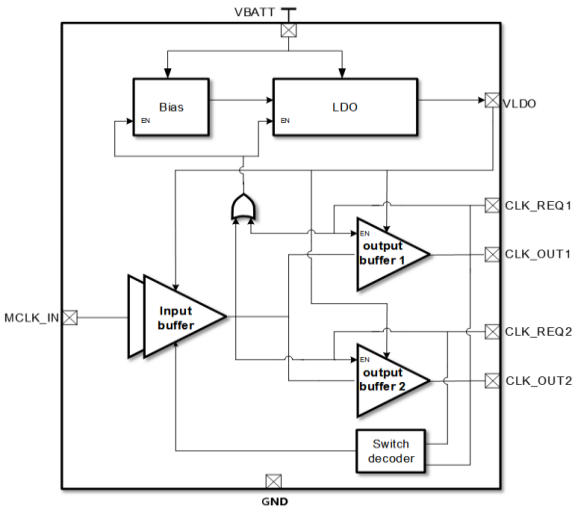
The chip accepts square waves or sine waves at the main clock input (MCLK_IN), with a minimum receivable sine wave signal of 0.3V (peak-to-peak).

This chip integrates a low-dropout regulator (LDO) that accepts an input voltage of 2.3V to 5.5V and provides a stable 1.8V, 50mA output to power peripherals.

It also supports level shifting, capable of converting clock levels from high to low (high level: 1.68～1.98V; low level: 1.08～1.32V).

The chip adopts a 0.4mm pitch wafer-level chip scale package (WLCSP: 0.78mm × 1.58mm).

Block Diagram



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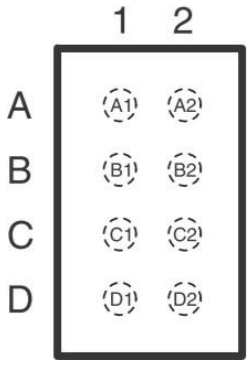
Pinout



I/O			
Pin	**Name**	**I/O**	**Description**
A1	V_{BATT}	I	Power
A2	CLK_OUT1	O	Clock Output1
B1	V_{LDO}	O	LDO output 1.8 V, as a power for internal modules.
B2	CLK_REQ1	I	Clock request signal 1, corresponding to CLK_OUT1
C1	MCLK_IN	I	Main clock input signal
C2	CLK_REQ2	I	Clock request signal 2, corresponding to CLK_OUT2
D1	GND	/	GND
D2	CLK_OUT2	O	Clock output2

Absolute Ratings					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Notes**
Power Supply	V_{BATT}	-0.3	7	V	
Input Voltage	CLK_REQ_1/2	-0.3	VBATT + 0.3	V	
	MCLK_IN	-0.3	1.98	V	
Output Voltage	V_{LDO}, CLK_OUT_1/2	-0.3	1.98	V	
Input Current	GND, VBATT, VLDO		±50	mA	
Output Current	CLK_OUT1/2		±20	mA	
Storage Temperature	Tstg	-55	150	°C	
Operating Temperature	T_A	-40	85	°C	
Junction Temperature	T_J	-40	150	°C	

Note: Exceeding the maximum absolute values specified in the table above may cause permanent damage to the chip. Long-term operation at maximum absolute values may affect chip lifespan and reliability.

Test conditions: -40℃≤TA≤85℃. It is recommended to operate the chip within the rated electrical range specified below.

Rated Parameters						
Parameter	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
Supply Voltage	V_{BATT}	2.3	3.3	5.5	V	/
Output Clock Voltage	CLK_OUT1/2	0	/	1.89	V	/
MCLK_IN Voltage	MCLK_IN	0	/	1.89	V	/
Input Control Voltage	CLK_REQ_1/2	0	/	3.6	V	/
Output Current	I_{OH}	-8	/	/	mA	/
	I_{OL}	/	/	8	mA	/

DC Parameters						
Parameters	Symbol	Value			Unit	Notes
		Min.	Typ.	Max.		
CLK_OUT1/2 Output High / Low Level	VOH1	1.44	1.8	/	V	Mode1, IOH = –8 mA
	VOH2	0.96	1.2	/	V	Mode2, IOH = –8 mA
	VOL	/	0	0.6	V	IOL = 8 mA
CLK_REQ_1/2 Input High / Low Level	VIH1	1.44	1.8	/	V	Mode1
	VIH2	2.7	3.3	/	V	Mode2
	VIL	/	0	0.36	V	/
MCLK_IN SWING	SW_{CLKIN}	0.3	1.8	1.89	V	Internally integrated AC coupling; supports sine wave or square wave input

Note: Test conditions: -40℃≤TA≤85℃

Power Consumption						
Parameters	Test Conditions	Min.	Typ.	Max.	Unit	Notes
I_{SB}	MCLK_IN=0Hz,CLK_REQ_1/2=0V	/	0.2	1	μA	/
I_{CCS}	MCLK_IN=0Hz,CLK_REQ_1/2=1.8V	/	0.4	1	mA	/
I_{OB}	f_{IN} = 26 MHz C_{Load} = 50 pF CLK_REQ_1=0V, CLK_REQ_2=1.8V or CLK_REQ_1=1.8V, CLK_REQ_2=0V	/	3.6	/	mA	/
C_{PD}	f_{IN} = 26 MHz	/	/	20	pF	Power dissipation capacitance

LDO Regulator							
Parameter	**Test Conditions**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
V_{OUT}	I_{OUT} = 50 mA		1.71	1.8	1.89	V	/
V_{LDO}	Mode2		1.08	1.2	1.32	V	External power supply
			1.62	1.8	1.98	V	
C_{LDO}	/		1	2.2	10	µF	External load capacitance
$I_{OUT(sc)}$	R_L = 0 Ω		/	100	/	mA	Output short-circuit current
$I_{OUT(pk)}$	V_{BATT} = 2.3 V , V_{LDO} = V_{OUT} − 5%		/	/	100	mA	Output peak current
PSR	V_{BATT} = 2.3 V	f_{IN} = 217 Hz and 1KHz	56	/	/	dB	Power supply rejection
	I_{OUT} = 2 mA	f_{IN} = 3.27 MHz	38	/	/	dB	
t_{su}	V_{BATT} = 2.3 V, C_{LDO} = 1 uF CLK_REQ_n to V_{IH} = 1.71 V		/	0.2	/	ms	LD start up time
	V_{BATT} = 5.5 V, C_{LDO} = 10 uF CLK_REQ_n to V_{IH} = 1.71 V		/	/	1	ms	

Clock Input Characteristics						
Parameters	**Test Conditions**	**Min**	**Typ**	**Max**	**unit**	**Notes**
I_I	V_I = 0, V_I = V_{IH}	/	/	1	µA	Leakage current for MCLK_IN, CLK_REQ1/2
C_I	f_{IN} = 26 MHz	/	0.9	/	pF	Input capacitance
R_I	f_{IN} = 26 MHz	/	4.8	/	kΩ	Input impedance
f_{IN}	/	10	26	80	MHz	Input frequency range

Clock Output Characteristics							
Parameter	**Test Conditions**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
Additional Phase Noise	f_{IN} = 26 MHz t_r/t_f ≤ 1 ns	1KHz offset	/	-139	/	dBc/Hz	/
		10KHz offset	/	-148	/		
		100KHz offset	/	-155	/		
		1MHz offset	/	-155	/		
Additional Jitter	f_{IN} = 26 MHz V_{pp} = 1.4V BW = 10 Hz − 5 MHz		/	0.31	/	ps （rms）	Mode1
	f_{IN} = 26 MHz V_{pp} = 1.4 V BW = 12KHz − 5 MHz		/	0.25	/	ps （rms）	Mode2
t_{DL}	/		/	11	/	ns	Propagation delay: from buffer input to output

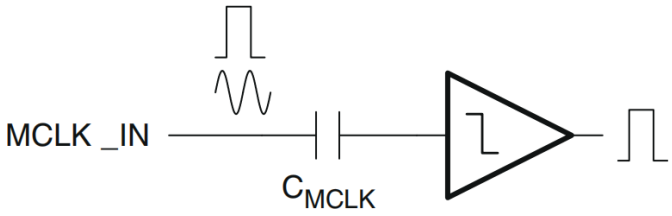
DC_L	f_{IN} = 26 MHz DC_{IN} = 50%	45%	50%	55%	/	Output duty cycle
t_r	C_L = 10 pF – 50 pF	1	/	5.2	ns	20% to 80% rise time
t_f	C_L = 10 pF – 50 pF	1	/	5.2	ns	20% to 80% fall time
t_{sk}	C_{L1} = C_{L2} = 10 pF – 50 pF	-0.5	/	0.5	ns	Inter-channel skew

Note: Test conditions: Sine wave clock source input

Functional Description

Support for Sine Wave and Square Wave Inputs:

The clock signal MCLK_IN supports sine wave or square wave inputs. CMCLK is an internal AC coupling capacitor, allowing direct connection to a TCXO without external capacitors. Any external components added in the series path of the clock signal may increase phase noise and jitter.



Chip-Integrated AC Coupling Capacitor

Internal LDO Power Supply:

This chip integrates a low-dropout (LDO) regulator that accepts an input voltage of 2.3V to 5.5V and provides a 1.8V, 50mA output. In Mode 1, the chip's core voltage is supplied by the internal integrated LDO. In Mode 2, the chip's core voltage requires an external power supply, input through the chip's VLDO pin.

Mode Switching and Chip Enable:

•Mode 1: The chip's core voltage is supplied by the 1.8V output of the internal integrated LDO.
•Mode 2: The chip's core voltage is supplied externally, with the VLDO pin serving as an external power input for the chip. The input voltage is typically 1.2V 1.8V, depending on user requirements. The chip enters Mode 2 when either CLK_REQ_1 or CLK_REQ_2 receives a voltage at VIH2 level.
•Standby Mode: When both external clock request signals are at low level, the internal LDO of the chip is turned off, and the chip enters a low-power standby mode with a standby current of 0.2μA, significantly reducing the power consumption of the application system.

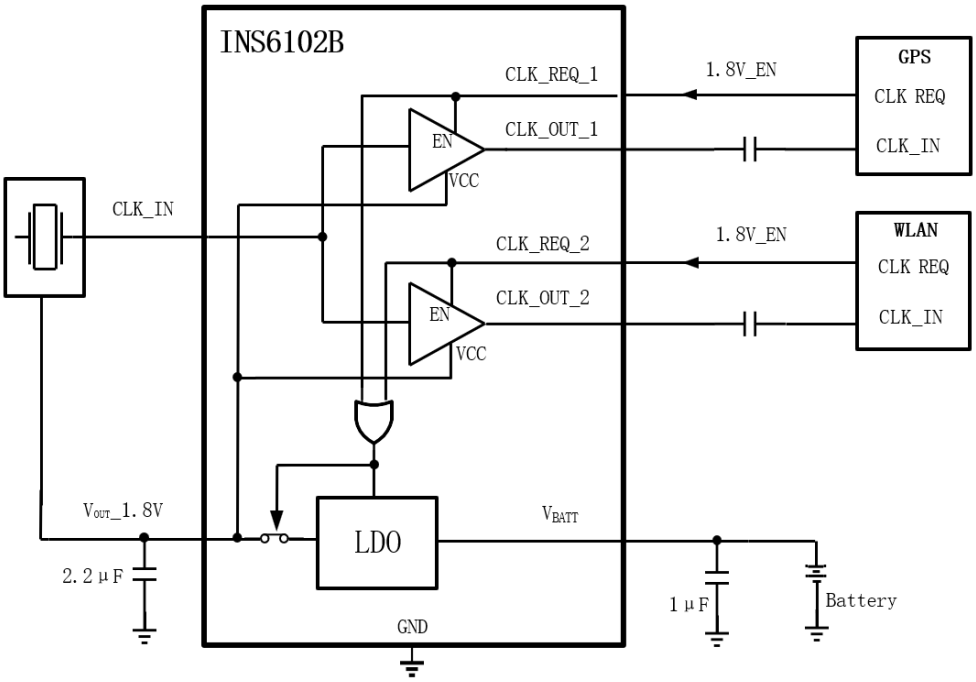
The internal output buffer and LDO module of the chip can be controlled based on the input voltage of the external request signal.

Definition of High/Low Levels for Request Signals				
Type	Symbol	Min	Max	Unit
V_{H1}	CLK_REQ_1/2	1.44	1.89	V
V_{H2}		2.7	3.6	V
V_L			0.36	V

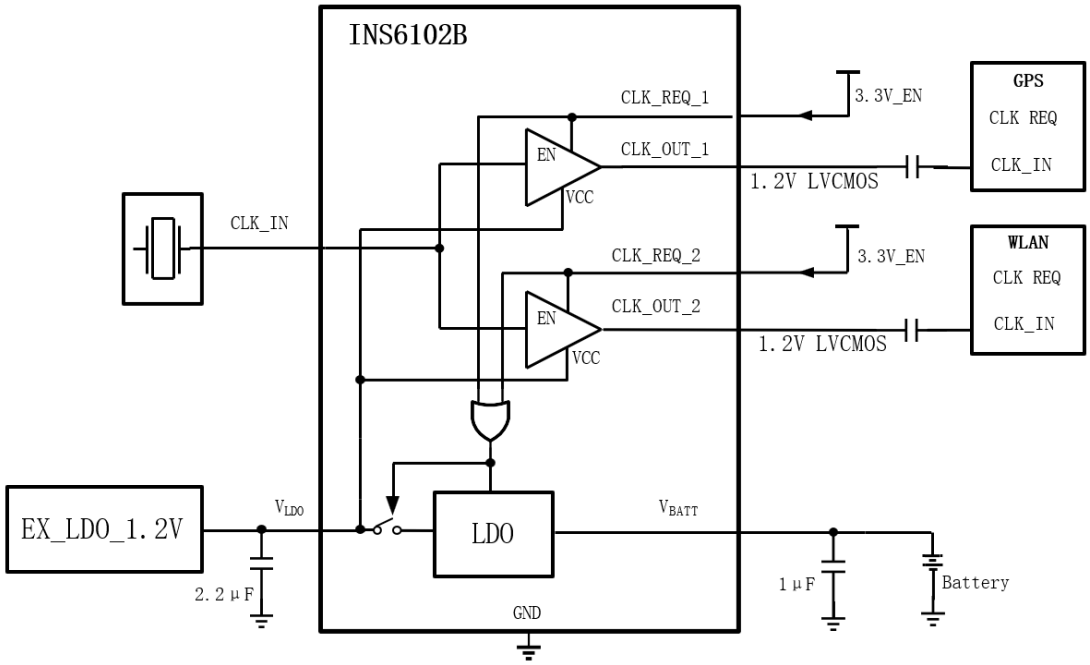
LDO Regulator States						
INPUTS			OUTPUTS		VLDO	Note
MCLK_IN	CLK_REQ1	CLK_REQ2	CLK_OUT1	CLK_OUT2		
X	V_L	V_L	L	L	X	Stand by Mode
CLK	V_L	V_{H1}	L	CLK	1.8V	Chip operates

Operating States						
CLK	V_{H1}	V_L	CLK	L	1.8V	In Mode 1
CLK	V_{H1}	V_{H1}	CLK	CLK	1.8V	
CLK	V_L	V_{H2}	L	CLK	Input VIO	Chip operates in Mode 2
CLK	V_{H2}	V_L	CLK	L	Input VIO	
CLK	V_{H2}	V_{H2}	CLK	CLK	Input VIO	

Typical Application 1 – Mobile Device



Typical Application 2 – Mobile Device



ACTINS6102B-PF

Low-Jitter Clock Buffer, WLCSP (0.8mm × 1.6mm), 8 pin, YFP 0.4mm

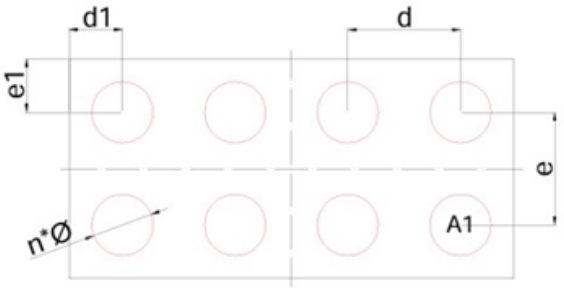
The chip has a wide variety of applications, including mobile phones, Global Positioning System (GPS), Wireless LAN, FM radio, WiMAX, and Wireless Bluetooth (W-BT). The above two typical application diagrams are examples for handheld mobile devices. In this application, a TCXO clock source is processed by the chip to drive a mobile GPS receiver or WLAN transceiver. Each CLK output channel is independently controlled by a separate clock request signal (CLK_REQ_1 or CLK_REQ_2) to enable clock output. When the chip enters standby mode, CLK_OUT_1 and CLK_OUT_2 are turned off, and the chip enters a low-power state. When any peripheral requests a clock, the ACTINS6102B-PF enables the LDO and powers the TCXO. The TCXO output (square wave, sine wave, or clipped sine wave) is converted to a square wave and buffered to the requested output.

Additional Specifications

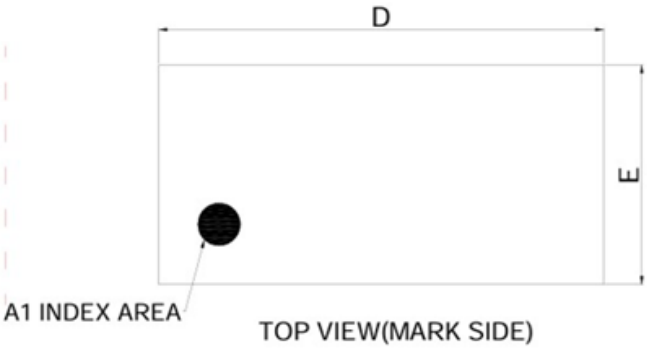
Parameters	Value	Unit	Notes
ESD Rating	±2000V	V	HBM，refer to ANSI/ESDA/JEDEC JS-001
	±1000V	V	CDM，refer to JEDEC specification JESD22-
Moisture Sensitivity Level	Level 3	/	/
RoHS Compliant	Yes	/	/

Package Specification

MIRROR REFLECT



BOTTOM VIEW(BALL SIDE)



TOP VIEW(MARK SIDE)

SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	ITEM	MIN	NOM	MAX
A	PACKAGE HEIGHT	0.429	0.464	0.499
A1	BALL HEIGHT	0.139	0.159	0.179
A2	WAFER THICKNESS	0.268	0.280	0.292
A3	DRY FILM THICKNESS	0.022	0.025	0.028
Φ	BALL DIAMETER	0.197	0.217	0.237
D	PACKAGE SIZE X	1.565	1.580	1.595
E	PACKAGE SIZE Y	0.765	0.780	0.795
d	MIN BALL PITCH X		0.400	
d1	MIN BALL CENTER TO PACKAGE SIZE X AXIS		0.190	
e	MIN BALL PITCH Y		0.400	
e1	MIN BALL CENTER TO PACKAGE SIZE Y AXIS		0.190	
n	BALL COUNT		8	

Drawing control: (Internal use only)
Commodity code: TBD
Issue number : N1
Date : 21/10/2025
Internal reference : D1

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